

BAD50 HR

DIS/UMA/Muxless Schematics Document

Sandy Bridge

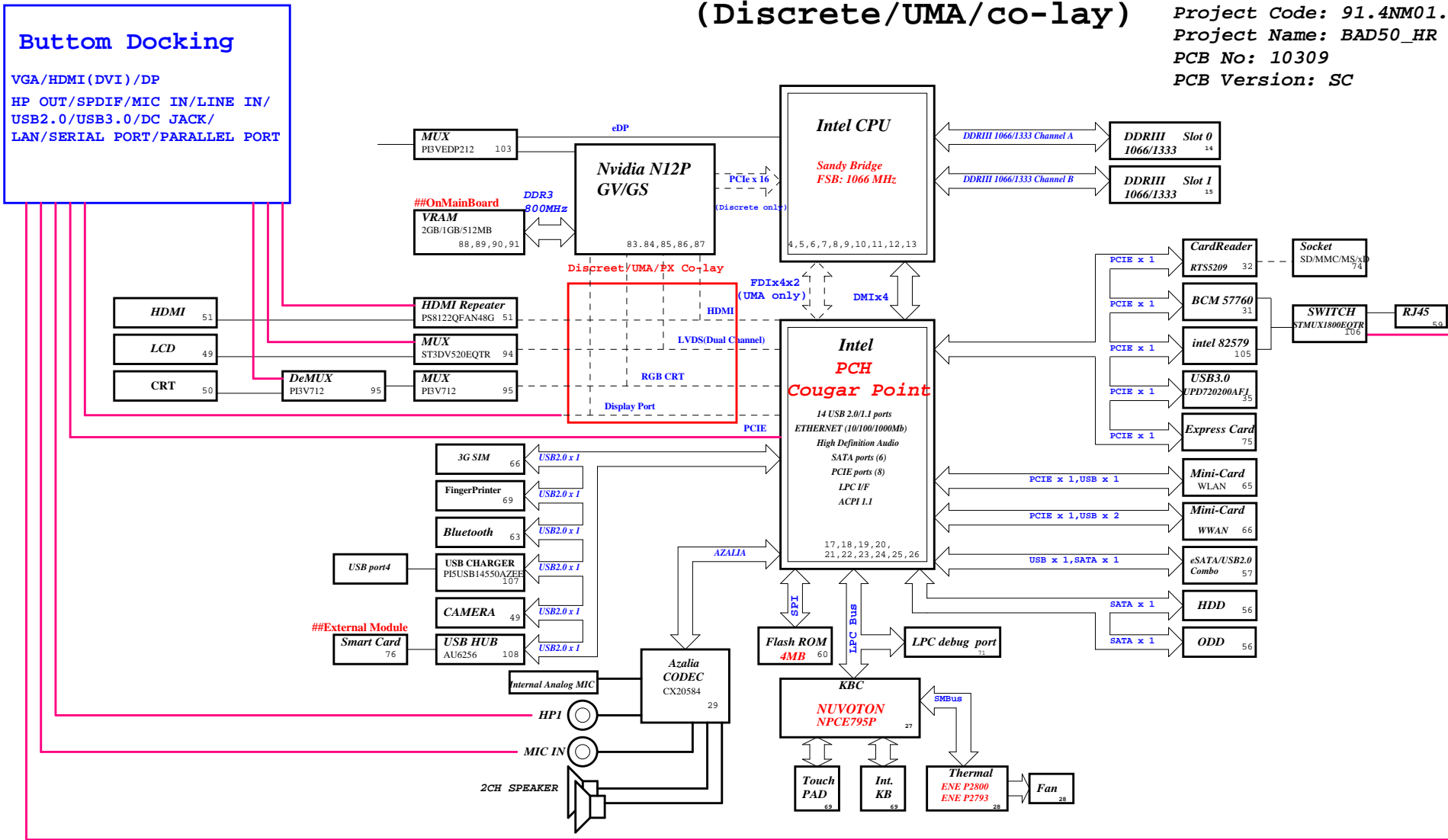
Intel PCH

DY :None Installed
DIS:DIS installed
DIS_Muxless :BOTH DIS or Muxless installed
DIS_PX:BOTH DIS or PX installed
DIS_PX_Muxless:DIS or PX or Muxless installed.
Muxless: Muxless installed.(PX4.0)
PX:MUX installed.(PX3.0)
PX_Muxless:BOTH PX or Muxless installed.
UMA:UMA installed
UMA_Muxless:BOTH UMA or Muxless installed
UMA_PX_Muxless:UMA or PX or Muxless installed

ANNIE: ONLY FOR ANNIE solution.
PSL: KBC795 PSL circuit for 10mW solution installed.
10mW: External circuit for 10mW solution installed.
65W: for 65W adaptor installed.
90W: for 90W adaptor installed.

BAD50-HR Block Diagram (Discrete/UMA/co-lay)

Project Code: 91.4NM01.001
Project Name: BAD50_HR
PCB No: 10309
PCB Version: SC



SYSTEM DC/DC	
TPS5146	48
INPUTS	OUTPUTS
5V_S5	0D85V_S0
CPU DC/DC	
VT1317SFCX	42-43
INPUTS	OUTPUTS
DCBATOUT	VCC_CORE
SYSTEM DC/DC	
RT8237AGQW	45
INPUTS	OUTPUTS
DCBATOUT	1D05V_VTT
SYSTEM DC/DC	
RT8239CGQW	41
INPUTS	OUTPUTS
DCBATOUT	5V_AUX_S5 3D3V_AUX_S5 5V_S5 3D3V_S5
SYSTEM DC/DC	
RT8207LGQW	46
INPUTS	OUTPUTS
DCBATOUT	1D5V_S3 0D75V_S0 0D6_VREF_S3
SYSTEM DC/DC	
VT1317SFCX	44
INPUTS	OUTPUTS
DCBATOUT	VCC_GFXCORE_PWR
VGA	
RT8208AGQW	92
INPUTS	OUTPUTS
DCBATOUT	VGA_CORE
TI CHARGER	
BQ24745RHR	40
INPUTS	OUTPUTS
DCBATOUT	BT+
SYSTEM DC/DC	
RT8015AGQW	47
INPUTS	OUTPUTS
3D3V_S5	1D8V_S0
3D3V_S0	3D3V_VGA_S0
SYSTEM DC/DC	
INPUTS	OUTPUTS
Switches	
INPUTS	OUTPUTS
1D5V_S3	1D5V_VGA_S0
3D3V_S0	3D3V_VGA_S0
PCB LAYER	
L1:Top	L5:Power
L2:GND	L6:Signal
L3:Signal	L7:GND
L4:Signal	L8:Bottom

Note:
Intel DMI supports both Lane Reversal and polarity inversion but only at PCH side. This is enabled via a soft strap.

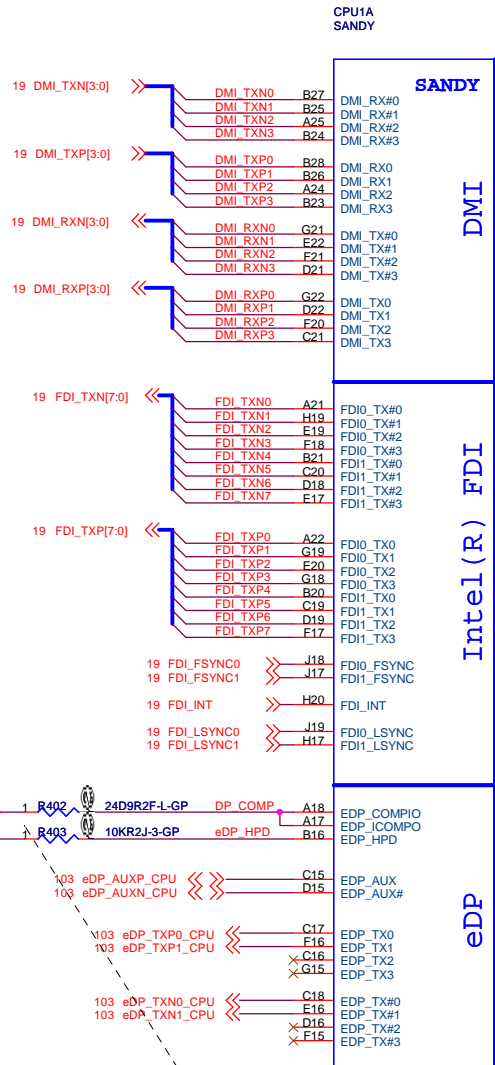
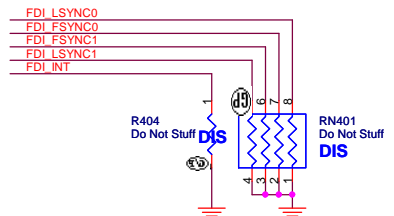
Note:
Intel FDI supports both Lane Reversal and polarity inversion but only at PCH side. This is enabled via a soft strap.

Note:
Lane reversal does not apply to FDI sideband signals.

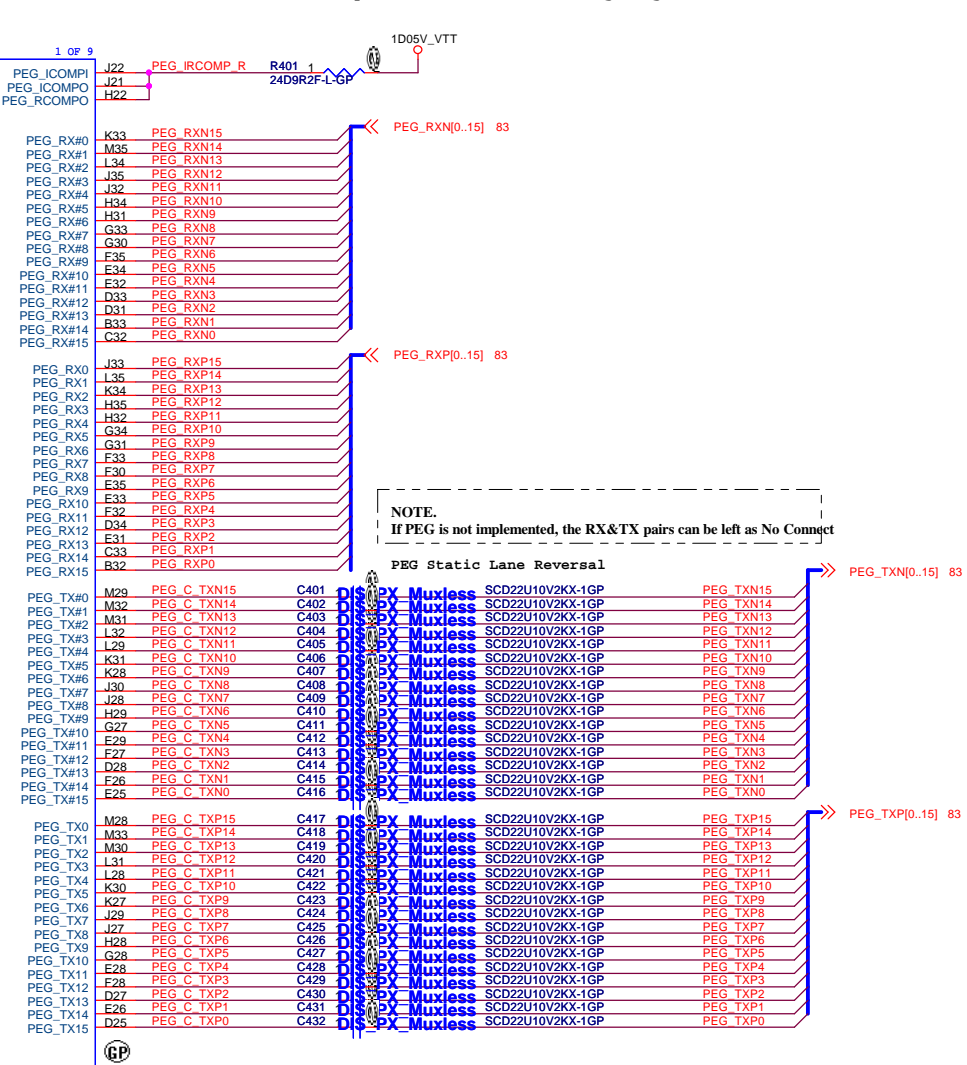
Signal Routing Guideline:
EDP_ICOMPO keep W/S=12/15 mils and routing length less than 500 mils.
EDP_COMPIO keep W/S=4/15 mils and routing length less than 500 mils.

NOTE:
Processor strap CFG[4] should be pulled low to enable Embedded DisplayPort.

Stuff to disable internal graphics function for power saving.

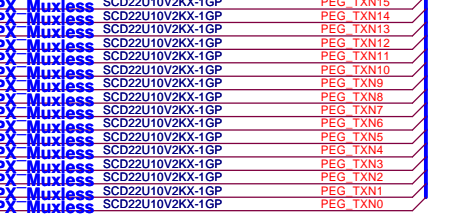


PCI EXPRESS* - GRAPHICS



NOTE:
If PEG is not implemented, the RX&TX pairs can be left as No Connect

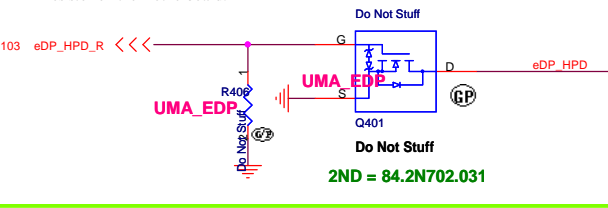
PEG Static Lane Reversal



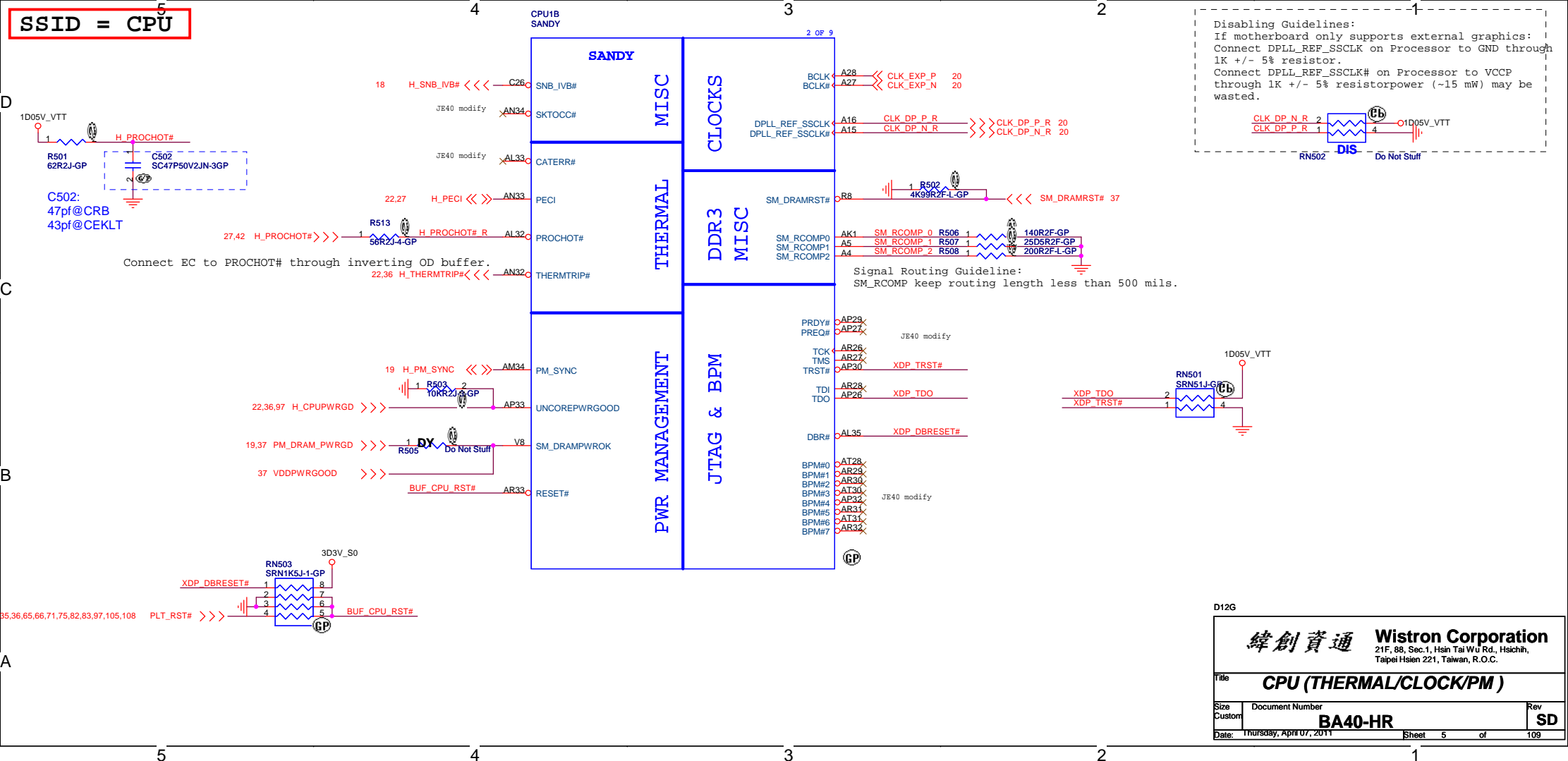
全改MUX

NOTE:
Select a Fast FET similar to 2N7002E whose rise/fall time is less than 6 ns. If HPD on eDP interface is disabled, connect it to CPU VCCIO via a 10-kΩ pull-Up resistor on the motherboard.

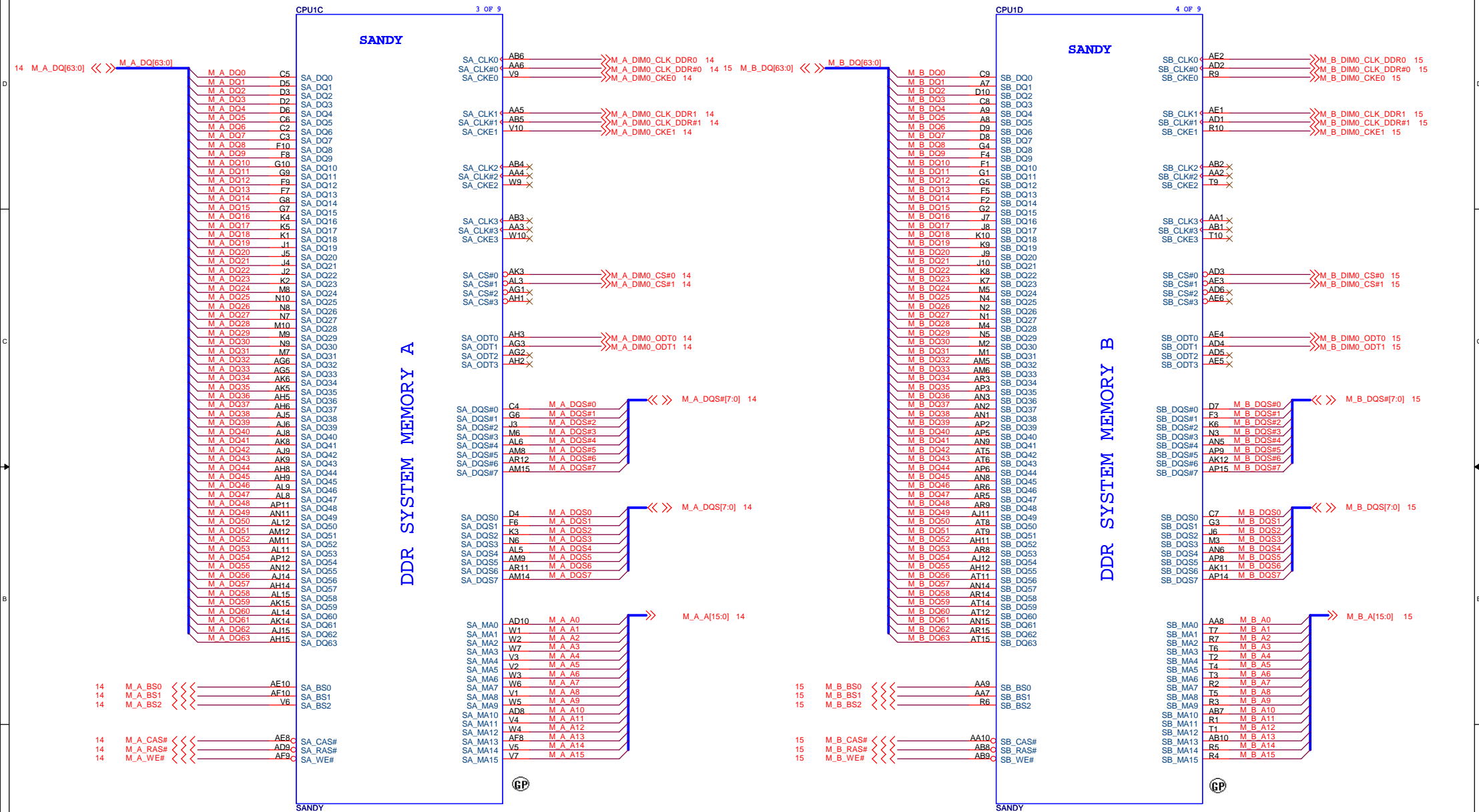
NOTE:
Select a Fast FET similar to 2N7002E whose rise/fall time is less than 6 ns. If HPD on eDP interface is disabled, connect it to CPU VCCIO via a 10-kΩ pull-Up resistor on the motherboard.



SSID = CPU

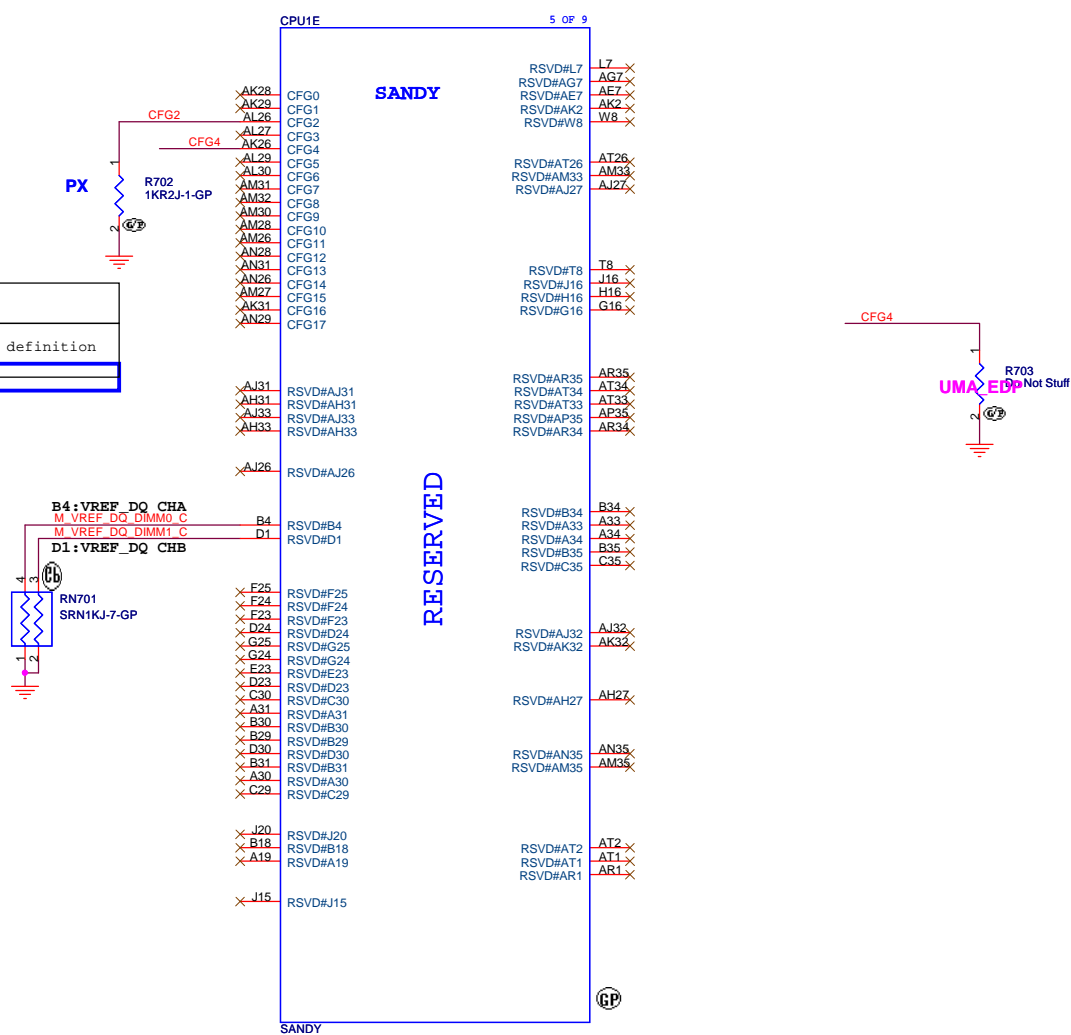


SSID = CPU



SSID = CPU

PEG Static Lane Reversal	
CFG2	1: Normal Operation; Lane # definition matches socket pin map definition
	0: Lane Reversed

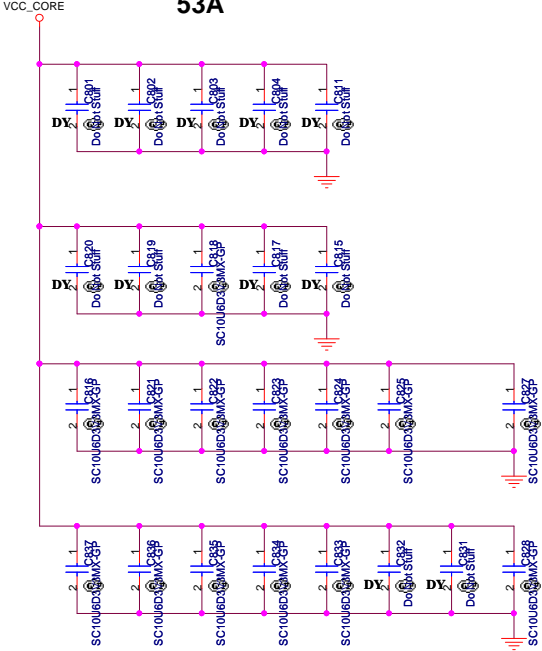


SSID = CPU

POWER

PROCESSOR CORE POWER

53A



VCC Output Decoupling Recommendation:
4 x 470 uF at Bottom Socket Edge
8 x 22 uF at Top Socket Cavity
8 x 22 uF at Top Socket Edge
8 x 22 uF at Bottom Socket Cavity

SANDY

VCC_CORE

- AG35 VCC
- AG34 VCC
- AG33 VCC
- AG32 VCC
- AG31 VCC
- AG29 VCC
- AG28 VCC
- AG27 VCC
- AG26 VCC
- AF35 VCC
- AF34 VCC
- AF33 VCC
- AF32 VCC
- AF31 VCC
- AF30 VCC
- AF29 VCC
- AF28 VCC
- AF27 VCC
- AF26 VCC
- AD35 VCC
- AD34 VCC
- AD33 VCC
- AD32 VCC
- AD31 VCC
- AD30 VCC
- AD29 VCC
- AD28 VCC
- AD27 VCC
- AD26 VCC
- AC35 VCC
- AC34 VCC
- AC33 VCC
- AC32 VCC
- AC31 VCC
- AC30 VCC
- AC29 VCC
- AC28 VCC
- AC27 VCC
- AC26 VCC
- AA35 VCC
- AA34 VCC
- AA33 VCC
- AA32 VCC
- AA31 VCC
- AA30 VCC
- AA29 VCC
- AA28 VCC
- AA27 VCC
- AA26 VCC
- Y35 VCC
- Y34 VCC
- Y33 VCC
- Y32 VCC
- Y31 VCC
- Y30 VCC
- Y29 VCC
- Y28 VCC
- Y27 VCC
- Y26 VCC
- U35 VCC
- U34 VCC
- U33 VCC
- U32 VCC
- U31 VCC
- U30 VCC
- U29 VCC
- U28 VCC
- U27 VCC
- U26 VCC
- R35 VCC
- R34 VCC
- R33 VCC
- R32 VCC
- R31 VCC
- R30 VCC
- R29 VCC
- R28 VCC
- R27 VCC
- R26 VCC
- P35 VCC
- P34 VCC
- P33 VCC
- P32 VCC
- P31 VCC
- P30 VCC
- P29 VCC
- P28 VCC
- P27 VCC
- P26 VCC

PEG AND DDR

CORE SUPPLY

SVID

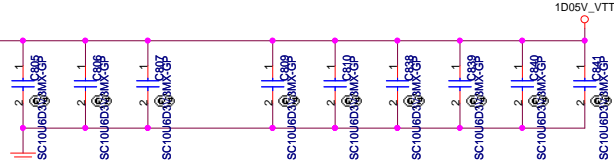
SENSE LINES

- VCCIO AH13
- VCCIO AH10
- VCCIO AG10
- VCCIO Y10
- VCCIO U10
- VCCIO P10
- VCCIO L10
- VCCIO J14
- VCCIO J13
- VCCIO J12
- VCCIO J11
- VCCIO H14
- VCCIO H12
- VCCIO H11
- VCCIO G14
- VCCIO G13
- VCCIO G12
- VCCIO F14
- VCCIO F13
- VCCIO F12
- VCCIO F11
- VCCIO F14
- VCCIO F12
- VCCIO E11
- VCCIO D14
- VCCIO D13
- VCCIO D12
- VCCIO D11
- VCCIO C14
- VCCIO C13
- VCCIO C12
- VCCIO C11
- VCCIO B14
- VCCIO B12
- VCCIO A14
- VCCIO A13
- VCCIO A12
- VCCIO A11
- VCCIO J23

- VIDALERT#
- VIDSCLK
- VIDSOUT

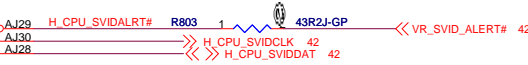
- VCC_SENSE
- VSS_SENSE
- VCCIO_SENSE
- VSSIO_SENSE

VCCIO Output Decoupling Recommendation:
2 x 330 uF (3 x 330 uF for 2012 capable designs)
5 x 22 uF & 5 x 0805 no-stuff at Bottom
7 x 22 uF & 2 x 0805 no-stuff at Top



No-stuff sites outside the socket may be removed.
No-stuff sites inside the socket cavity need to remain.

For CRB VIDSOUT need to pull high 130 ohm close to CPU and IMV/P7
For CRB VIDALERT# need to pull high 75 ohm close to CPU



VCC_CORE

R801,R802 close to CPU



D12G

偉創資通 Wistron Corporation
21F, 88, Sec.1, Hsin-Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

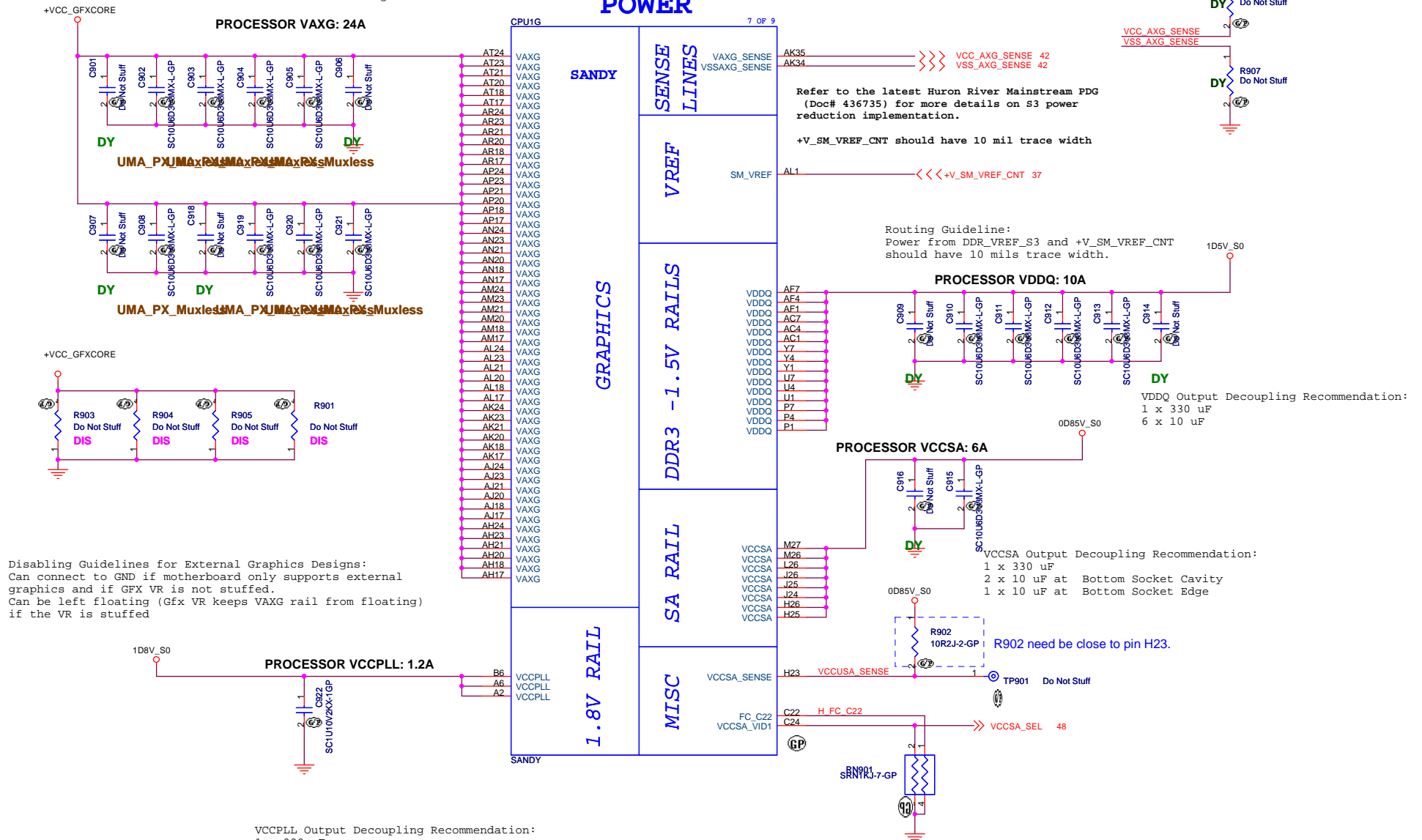
Title CPU (VCC_CORE)
Size Custom Document Number BA40-HR Rev SD
Date: Thursday, April 07, 2011 Sheet 8 of 109

WWW.ALISALER.COM

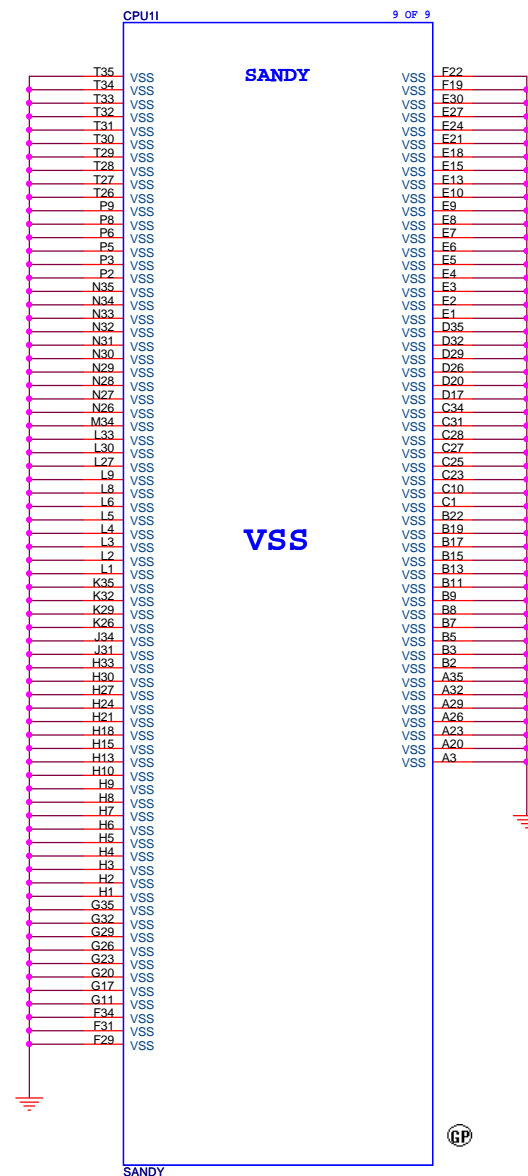
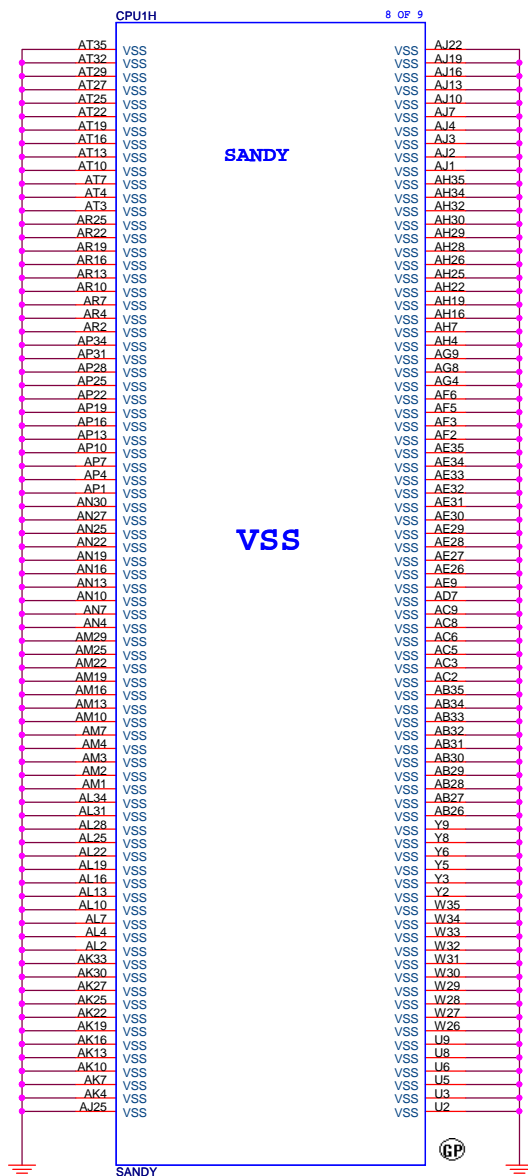
VCCPLL Output Decoupling Recommendation:

- 1 x 330 uF
- 2 x 1 uF
- 1 x 10 uF

Title			
CPU (VCC GFXCORE)			
Size A3	Document Number		Rev
	BA40-HR		SD
Date:	Thursday, April 07, 2011	Sheet 9 of 109	



SSID = CPU



WWW.ALISALER.COM

JE40 delete XDP function

D12G

緯創資通

Wistron Corporation

21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

XDP

Size
A3

Document Number
BA40-HR

Rev
SD

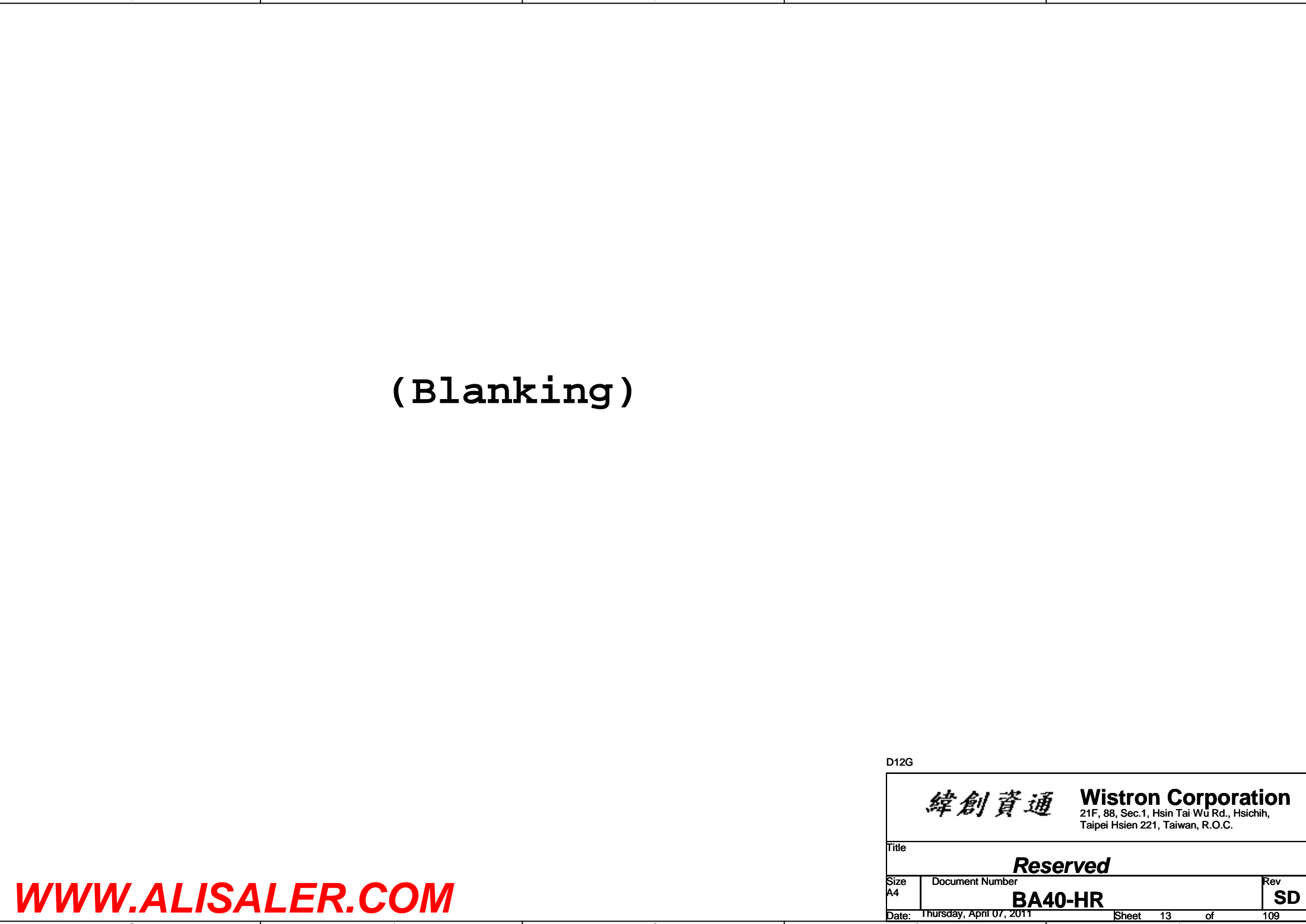
Date: Thursday, April 07, 2011

Sheet 11 of 109

(Blanking)

D12G

<div>緯創資通</div> <div>Wistron Corporation</div> <div>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</div>		
Title <div>Reserved</div>		
Size <div>A4</div>	Document Number <div>BA40-HR</div>	Rev <div>SD</div>
Date: Thursday, April 07, 2011		Sheet 12 of 109

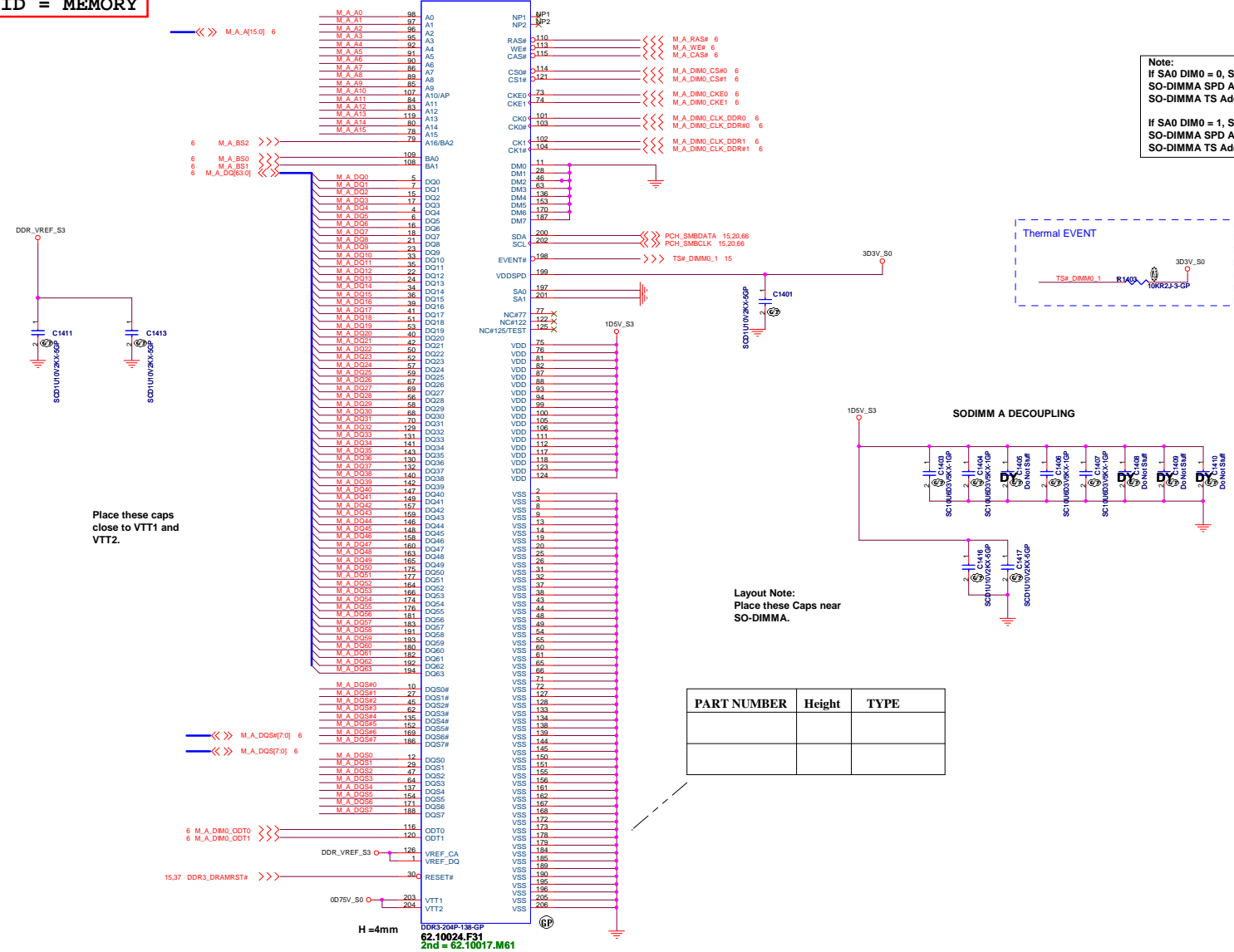


(Blanking)

WWW.ALISALER.COM

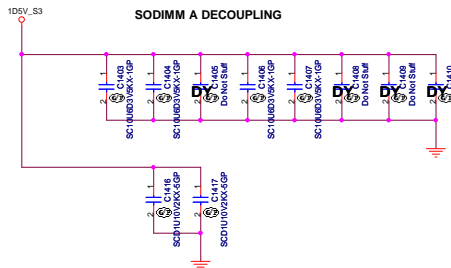
D12G			
緯創資通		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
Reserved			
Size A4	Document Number BA40-HR		Rev SD
Date:	Thursday, April 07, 2011	Sheet 13 of	109

SSID = MEMORY



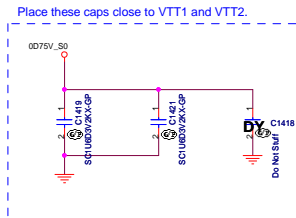
Note:
If SA0_DIM0 = 0, SA1_DIM0 = 0
SO-DIMMA SPD Address is 0xA0
SO-DIMMA TS Address is 0x30

If SA0_DIM0 = 1, SA1_DIM0 = 0
SO-DIMMA SPD Address is 0xA2
SO-DIMMA TS Address is 0x32

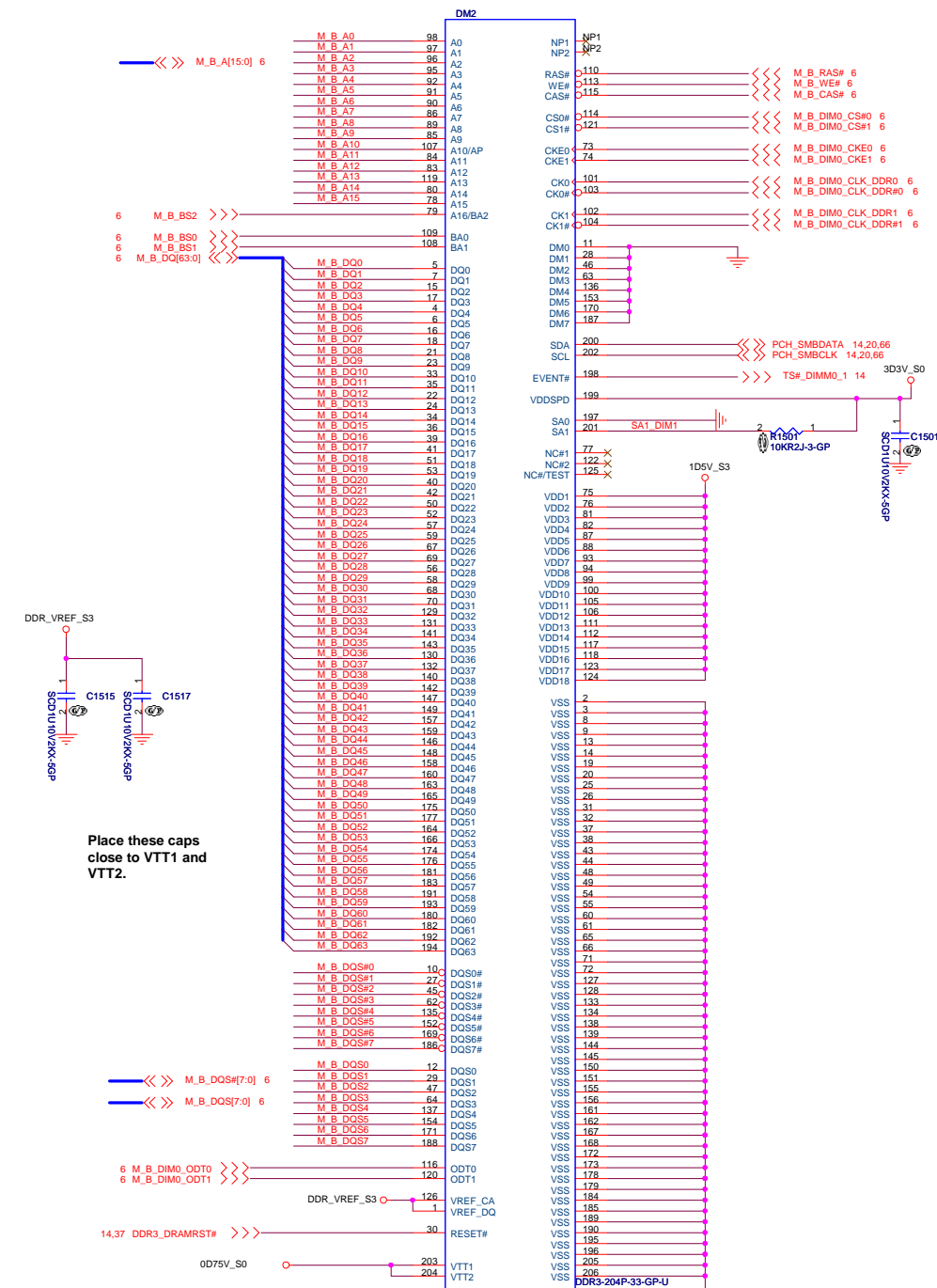


Layout Note:
Place these Caps near
SO-DIMMA.

PART NUMBER	Height	TYPE



SSID = MEMORY

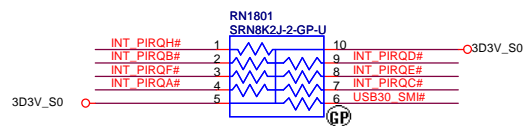


(Blanking)

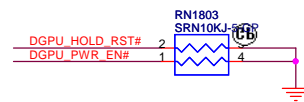
D12G

<div>緯創資通</div> <div>Wistron Corporation</div> <div>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</div>		
Title <div>DDR3-SODIMM2</div>		
Size <div>A4</div>	Document Number <div>BA40-HR</div>	Rev <div>SD</div>
Date: Thursday, April 07, 2011		Sheet 16 of 109

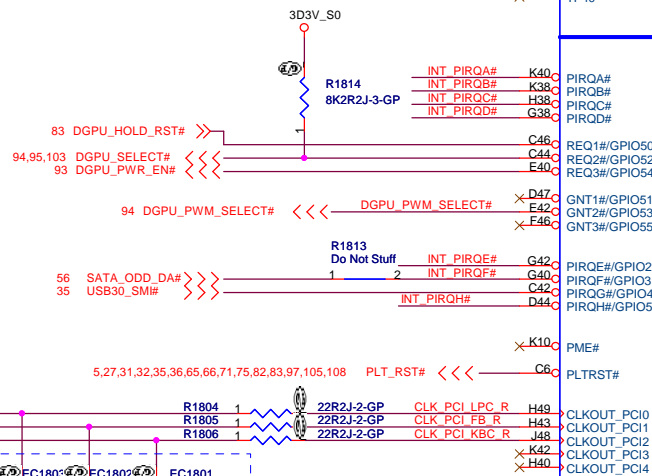
SSID = PCH



A16 swap override Strap/Top-Block Swap Override jumper	
PCI_GNT#3	Low = A16 swap override/Top-Block Swap Override enabled High = Default

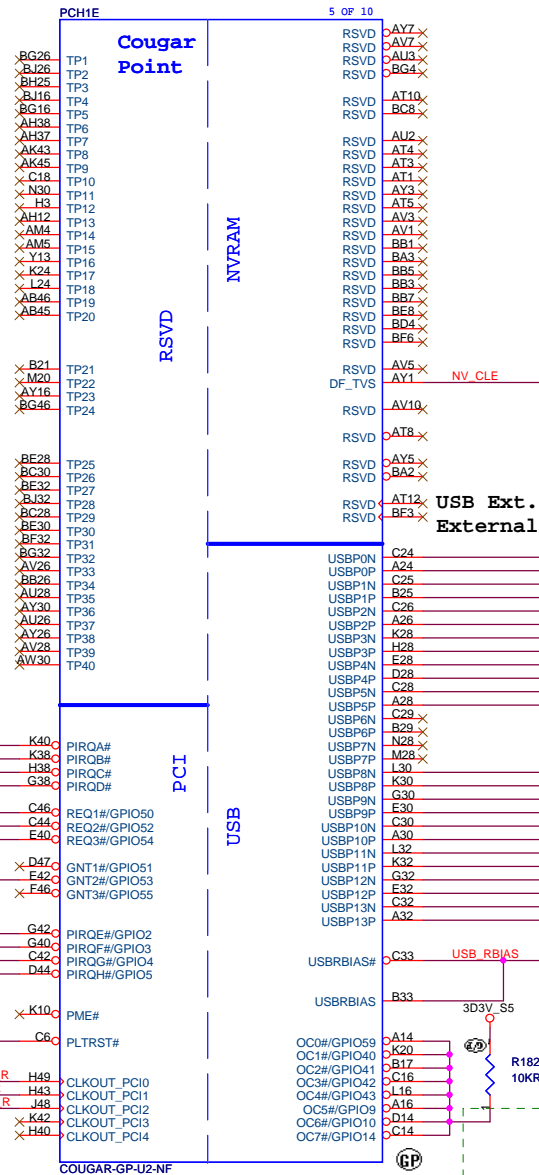


BOOT BIOS Strap		
GNT1#/GPIO51	SATA1GP/GPIO19	BOOT BIOS Location
0	0	LPC
0	1	Reserved
1	0	Reserved
1	1	SPI(Default)



-1_0303

^lEMI request 20101109



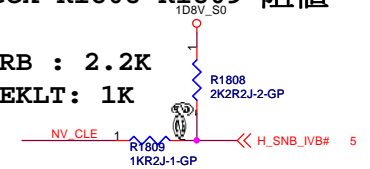
OC[3:0]# for Device 29 (Ports 0-7)
OC[7:4]# for Device 26 (Ports 8-13)

-1_0317

check R1808 R1809 阻值

CRB : 2.2K

CEKLT: 1K



DMI & FDI Termination Voltage

NV_CLE	Set to Vss when LOW
	Set to Vcc when HIGH

~~2~~ USB Ext. port 1 (HS)

* External debug port use on Huron river platform

USB Table

Pair	Device
0	3G Card
1	USB port1(SATA Combo), on M/B
2	Fingerprint
3	BLUETOOTH
4	Mini Card2 (WWAN)
5	Dock
6	X
7	X
8	USB port4 on S/B(usb charger)
9	USB port 2 on S/B
10	USB port 3 (only when 3.0 not support)
11	Mini Card1 (WLAN)
12	CAMERA
13	New Card or USB HUB(New/Smart)

USB 2.0 Overcurrent Pin Default Usage

Pin	Default Port Mapping	Pin	Default Port Mapping
OC0#	Port 0, Port 1	OC4#	Port 8, Port 9
OC1#	Port 2, Port 3	OC5#	Port 10, Port 11
OC2#	Port 4, Port 5	OC6#	Port 12, Port 13
OC3#	Port 6, Port 7	OC7#	Not Used

D12G

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	PCH (PCI/USB/NVRAM)
-------	----------------------------

Size A3	Document Number BA40-HR	Rev SD
Date: Thursday, April 07, 2011		Sheet 18 of 109

SSID = PCH

Signal Routing Guideline:
DMI_ZCOMP keep W=4 mils and
routing length less than 500
mils.
DMI_IRCOMP keep W=4 mils and
routing length less than 500
mils.



PCH1C

Cougar
Point

3 OF 10



Deep S4/S5 Supported

Deep S4/S5 Not Supported

VccDSW3_3

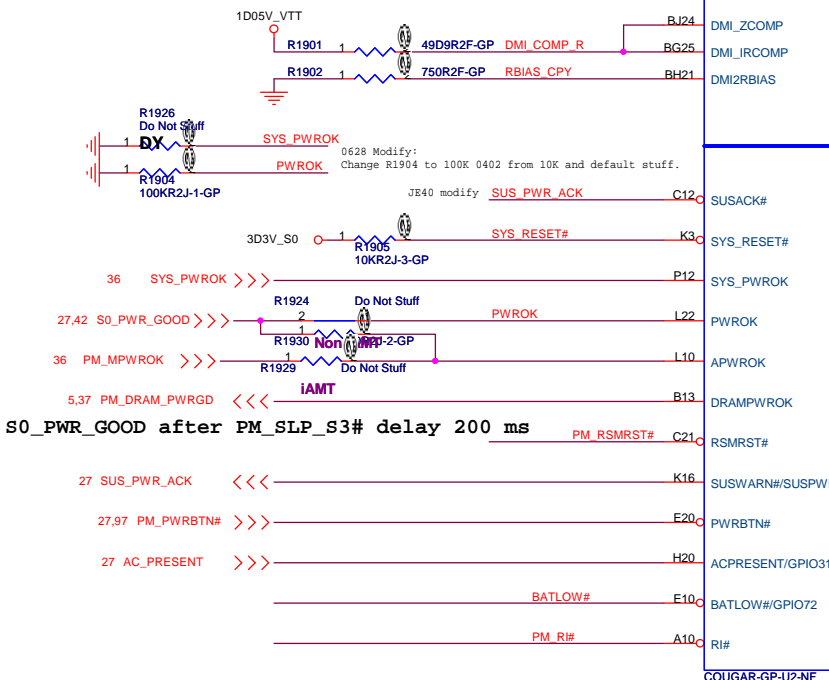
DPWROK

VccSUS3_3

RSMRST#

For platforms not supporting Deep S4/S5

- 1.VccSUS3_3 and VccDSW3_3 will rise at the same time (connected on board)
- 2.DPWROK and RSMRST# will rise at the same time (connected on board)
- 3.SLP_SUS# and SUSACK# are left as 'no connect'
- 4.SUSWARN# used as SUSPWRDNACK/GPIO30



S0_PWR_GOOD after PM_SLP_S3# delay 200 ms

System Power Management



DSWVRMEN

DPWROK

WAKE#

CLKRUN#/GPIO32

SUS_STAT#/GPIO61

SUSCLK/GPIO62

SLP_S5#/GPIO63

SLP_S4#

SLP_S3#

SLP_A#

SLP_SUS#

PMSYNCH

SLP_LAN#/GPIO29

GP

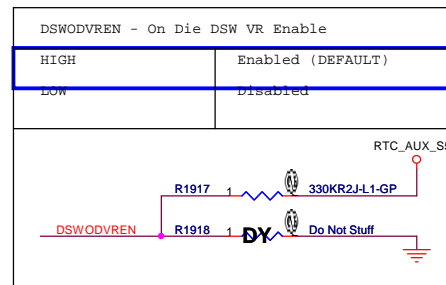
GP

GP

GP

GP

GP



PWRBTN#
This signal has an internal pull-up resistor

PM_RSMRST#

CRB : PL 10K

NNN : PL 10K

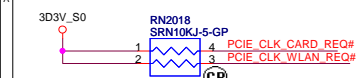
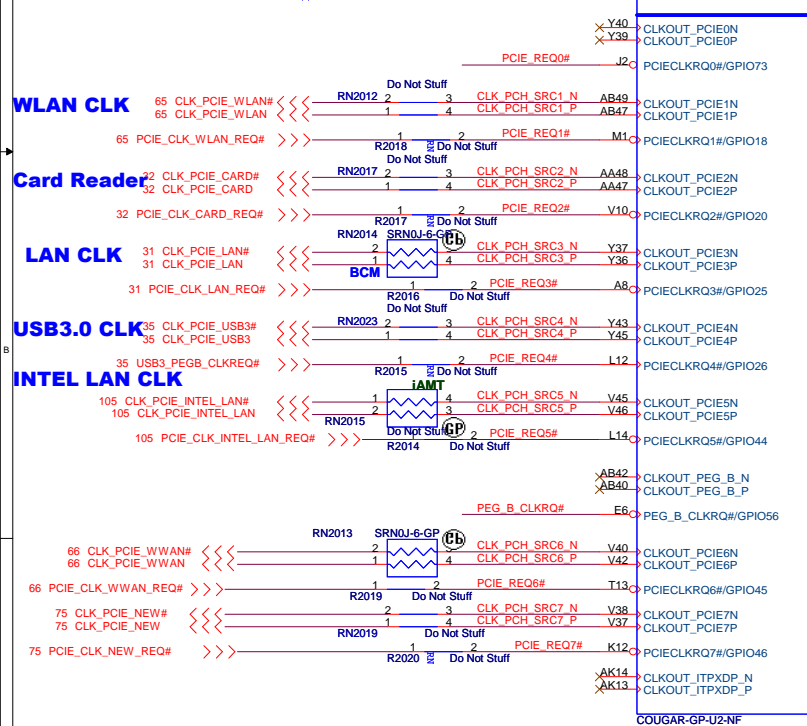
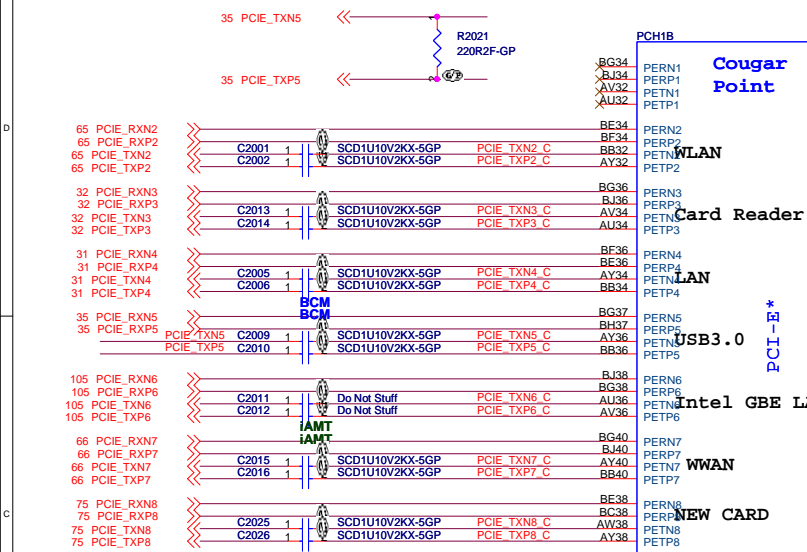
WWW.ALISALER.COM

D12G

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

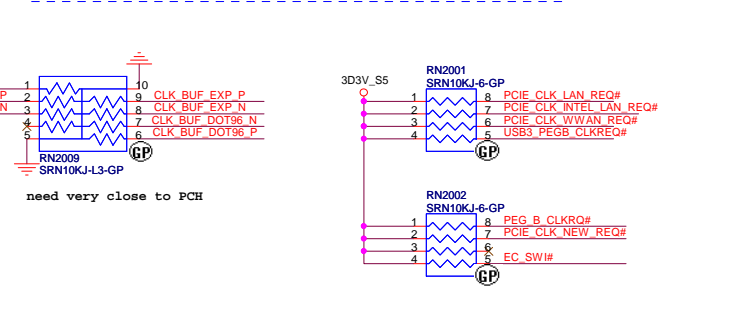
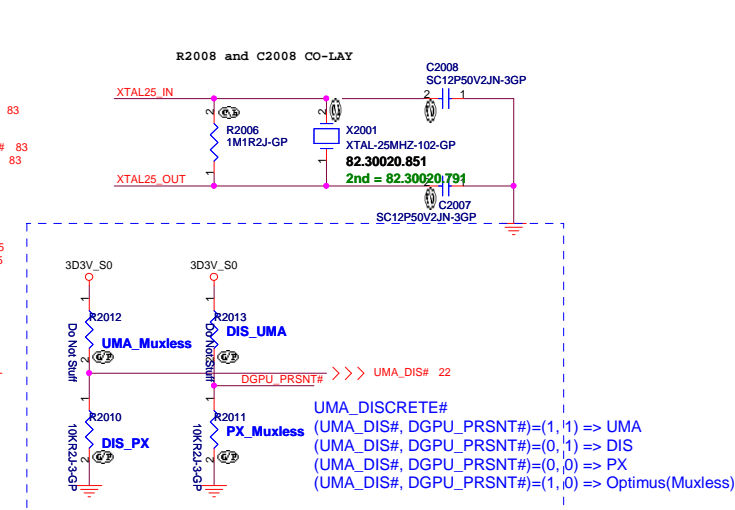
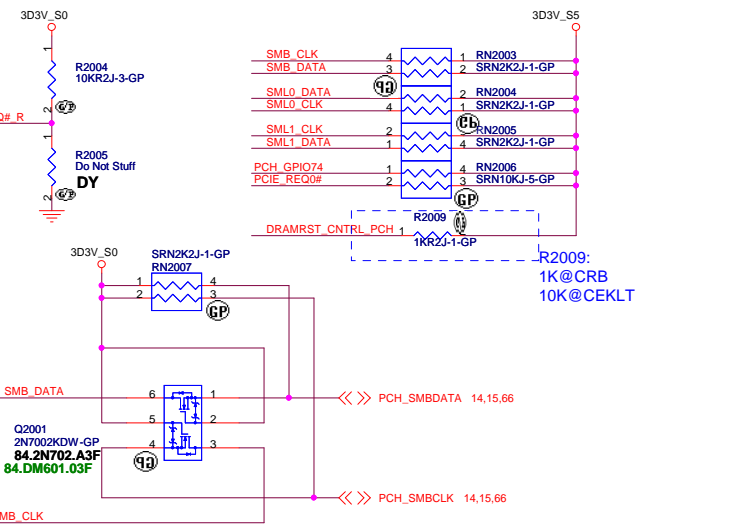
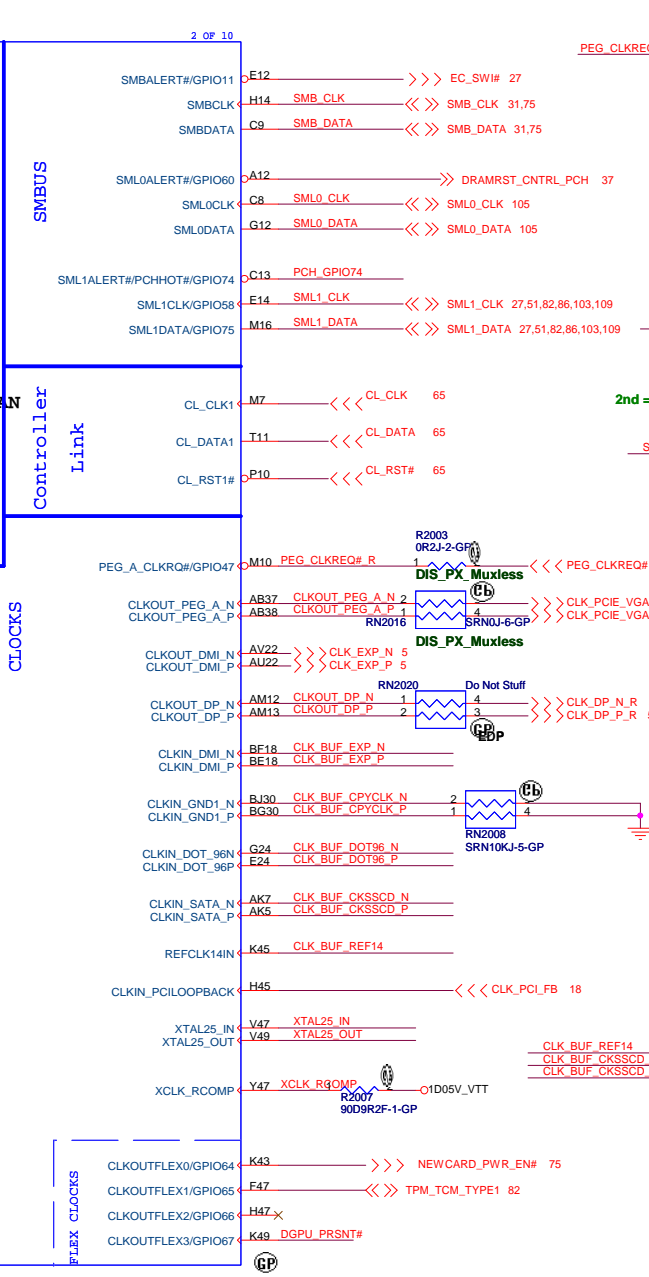
Title PCH (DM I/FDI/PM)
Size A3 Document Number BA40-HR
Date Thursday, April 07, 2011 Sheet 19 of 109
Rev SD

SSID = PCH



PCIECLKRQ1# and PCIECLKRQ2#
Support S0 power only

WWW.ALISALER.COM



- Prioritize 27/14/24/48/25-MHz FLEX on FLEX1 and FLEX3
- Do not configure 27/14/24/48/25-MHz FLEX clock on FLEX0 and FLEX2 if more than 2 PCI clocks + PCI loopback are routed.

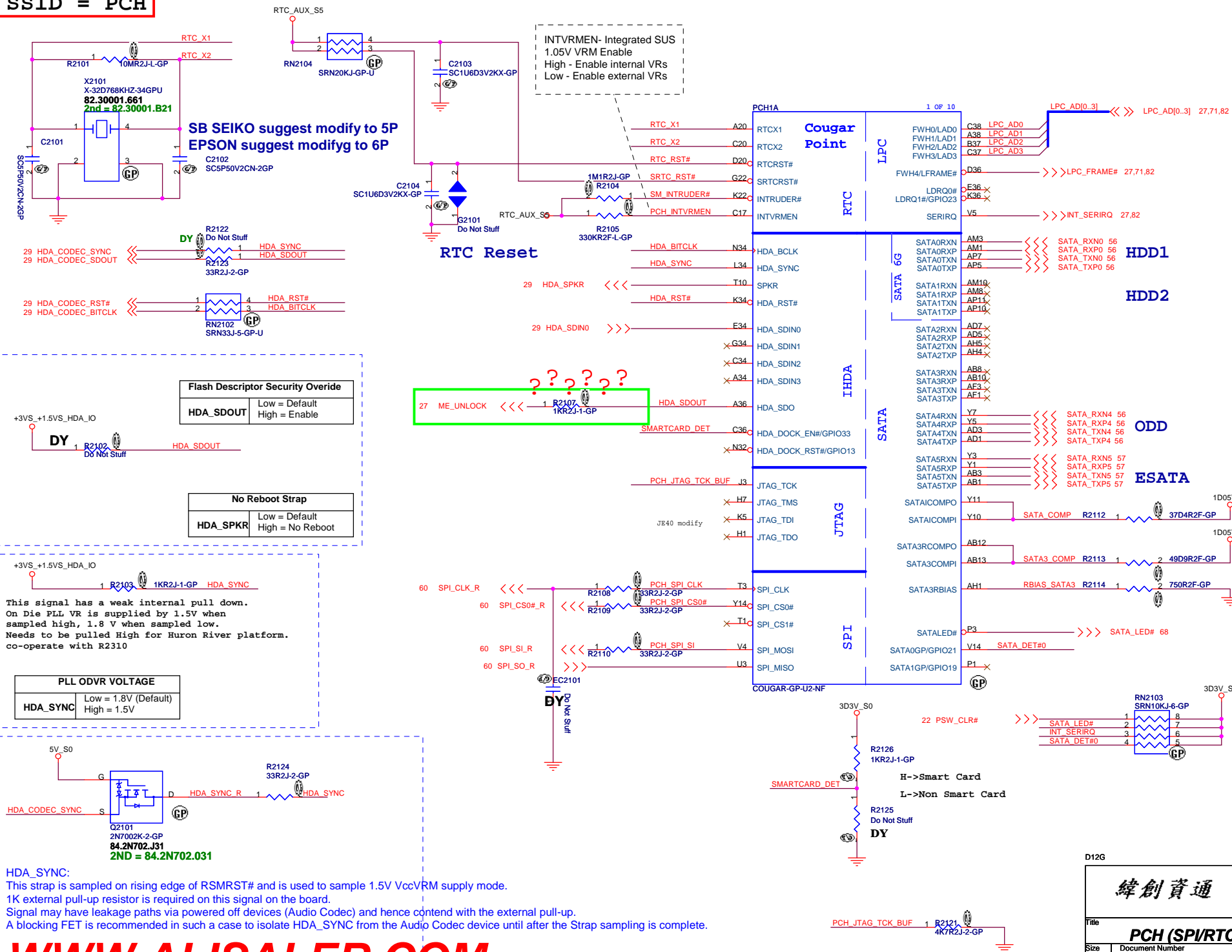
D12G

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

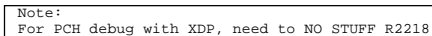
Title
PCH (PCI-E/SMBUS/CLOCK/CL)

Size	Document Number	Rev
Custom	BA40-HR	S
Date:	Thursday, April 07, 2011	Sheet 20 of 109

SSID = PCH



WWW.ALISALER.COM



3D3V_S0

1 2 3 4

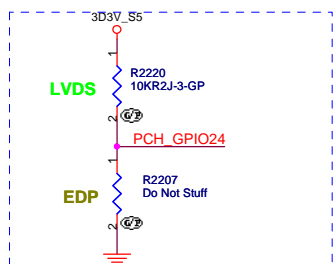
RN2203

SRN10KJ-5-GP

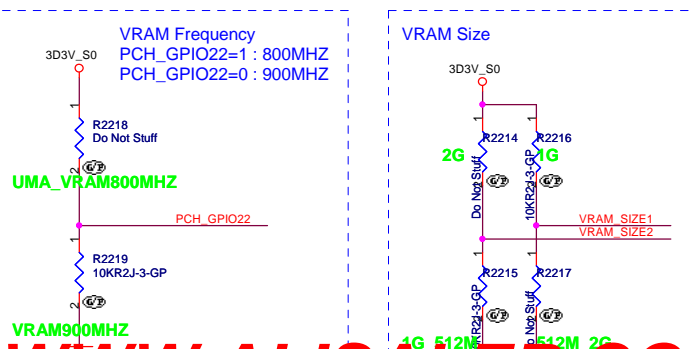
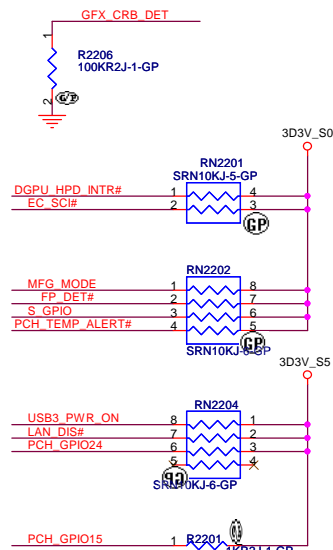
GP

H_RCIN#
H_A20GATE

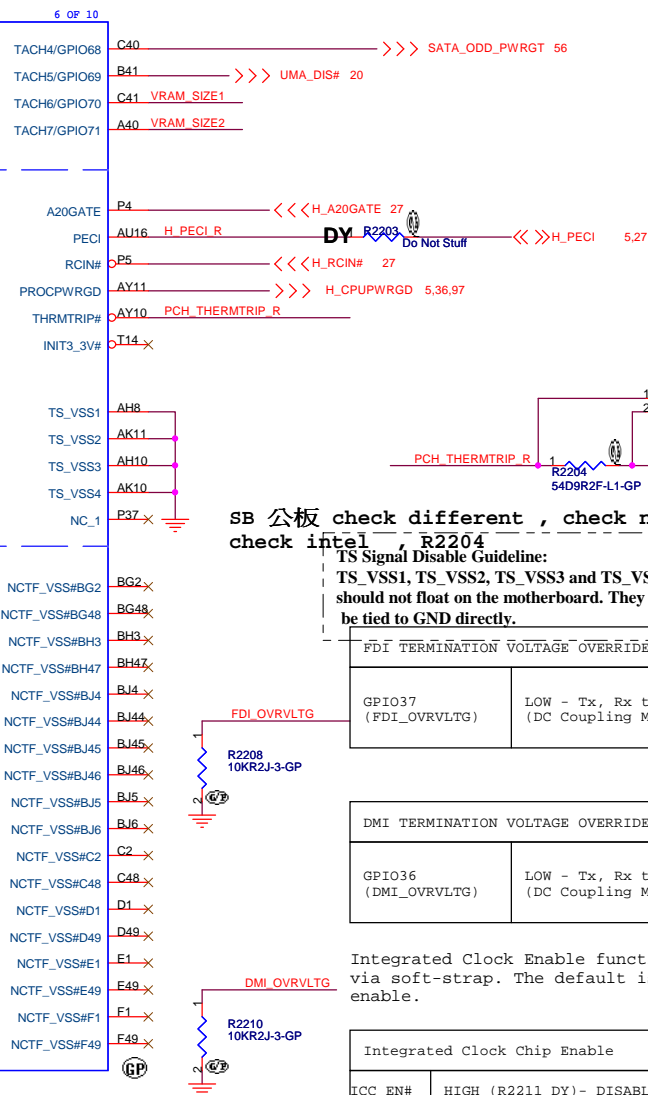
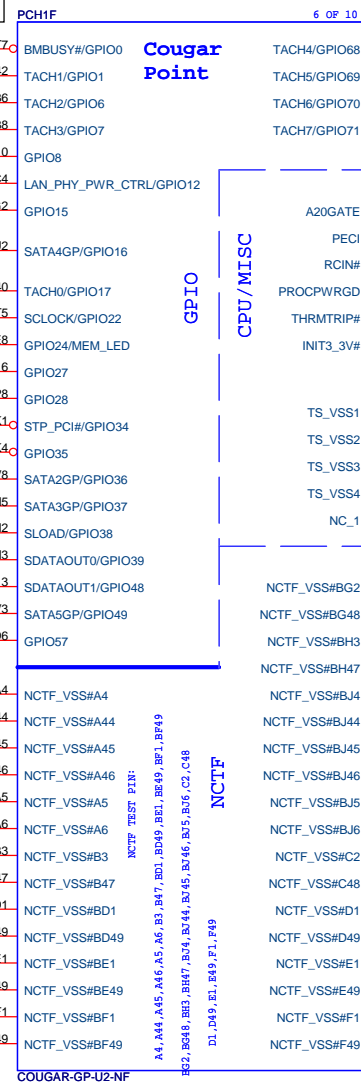
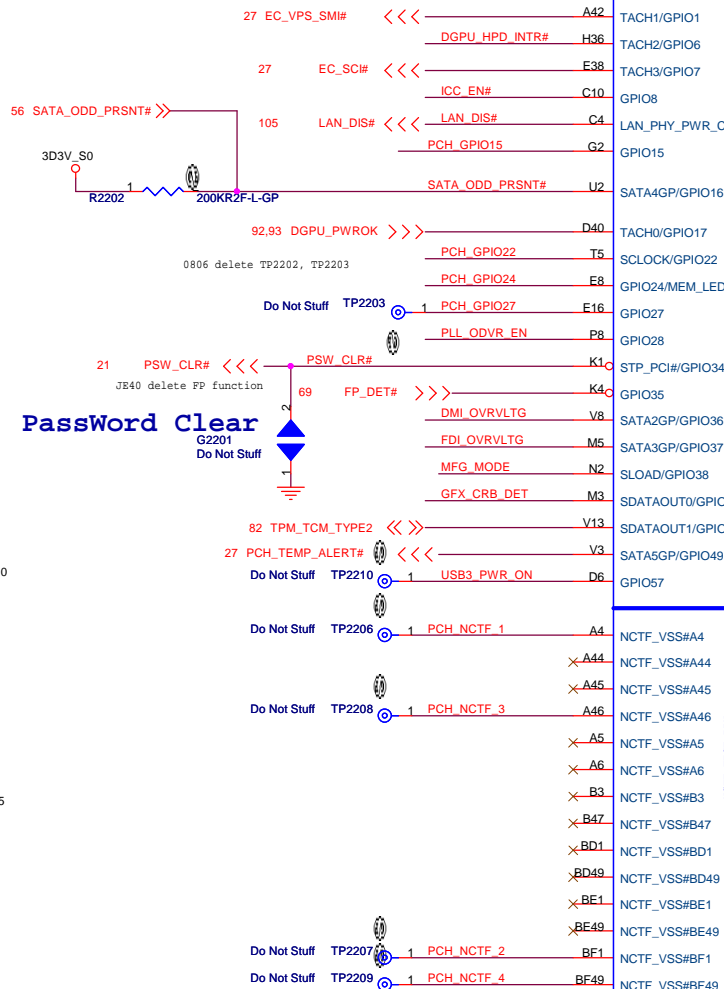
GPIO27 has a weak[20K] internal pull up.
To enable on-die PLL Voltage regulator,
should not place external pull down.



	INTERNAL GFX	EXTERNAL GFX
R2205	DY	10K
R2206	100K	DY



WWW.ALISALER.COM



SB 公板 check different , check need modify or not
check intel , R2204

TS Signal Disable Guideline:

TS_VSS1, TS_VSS2, TS_VSS3 and TS_VSS4 should not float on the motherboard. They should be tied to GND directly.

FDI TERMINATION VOLTAGE OVERRIDE	
GPIO37 (FDI_OVRVLTG)	LOW - Tx, Rx terminated to same voltage (DC Coupling Model DEFAULT)

DMI TERMINATION VOLTAGE OVERRIDE	
GPIO36 (DMI_OVRVLGTG)	LOW - Tx, Rx terminated to same voltage (DC Coupling Model DEFAULT)

Integrated Clock Enable functionality is achieved via soft-strap. The default is integrated clock enable.

Integrated Clock Chip Enable	
ICC_EN#	HIGH (R2211 DY)- DISABLED [DEFAULT] LOW (R2211)- ENABLED

GPIO8 has a weak[20K] internal pull up.
Integrated Clock Enable functionality is achieved
via soft-strap. The default is integrated clock
enable.

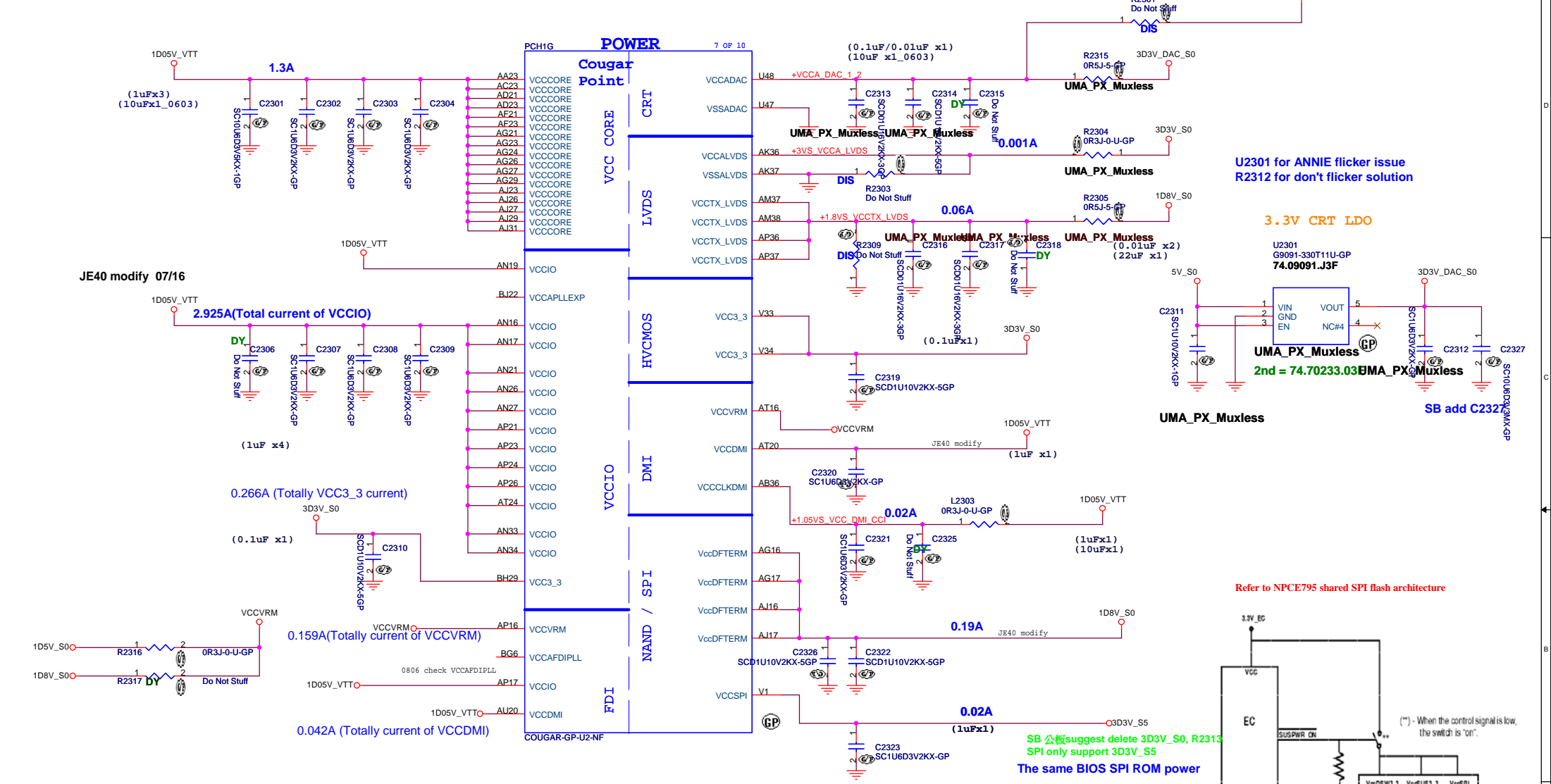
PLL ON DIE VR ENABLE
NOTE: This signal has a weak internal pull-up 20kΩ. ENABLED -- HIGH (R2212 UNSTUFFED) DEFAULT DISABLED -- LOW (R2212 STUFFED)

PLL ODVR_EN DY 1 R2212 Do Not Stuff

D12G

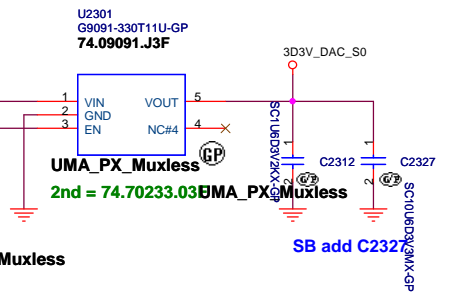
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title			
PCH (GPIO/CPU)			
Size A3	Document Number		Rev
	BA40-HR		S
Date:	Thursday, April 07, 2011	Sheet 22 of	109

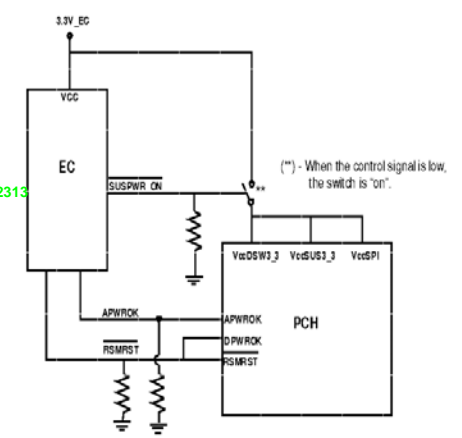


U2301 for ANNIE flicker issue
R2312 for don't flicker solution

3.3V CRT LDO

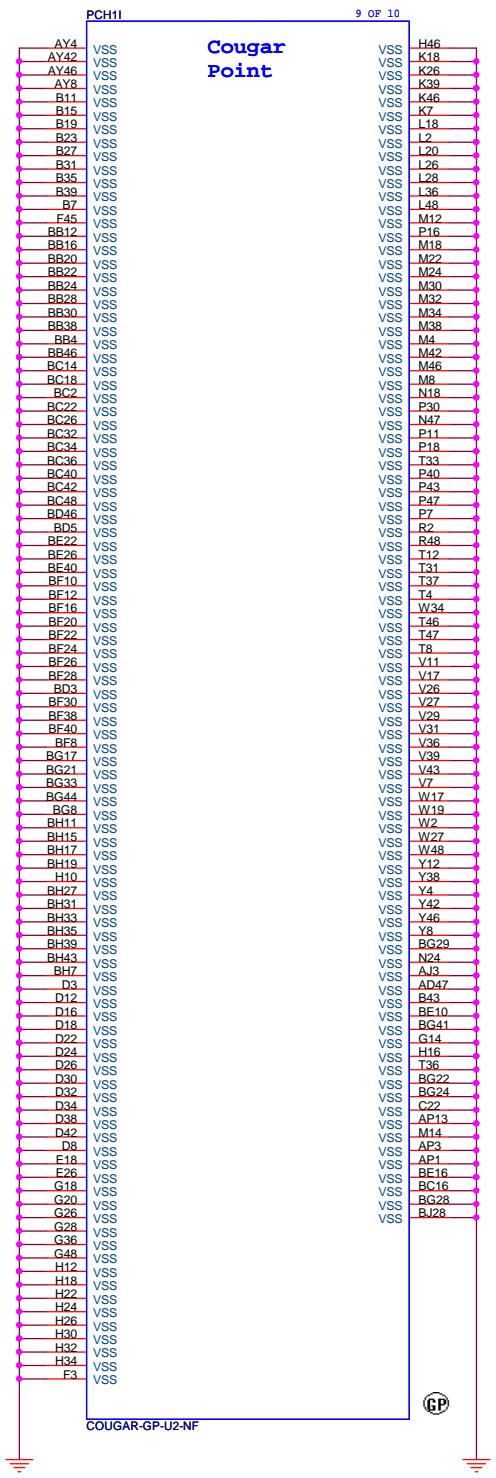
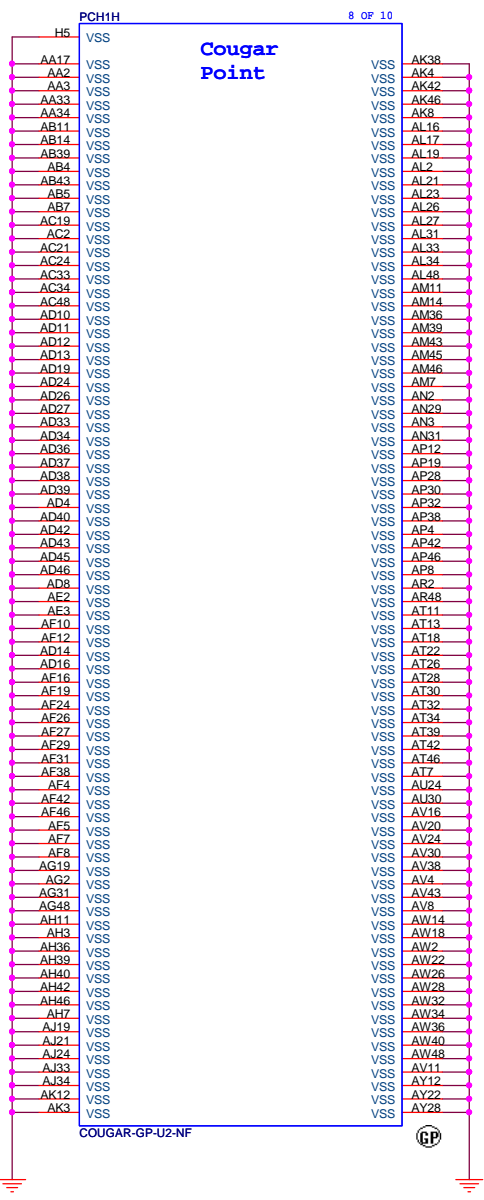


Refer to NPCE/795 shared SPI flash architecture





SSID = PCH



WWW.ALISALER.COM

D12G

緯創資通 Wistron Corporation

21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title PCH (VSS)

Size A3 Document Number BA40-HR Rev SD

Date: Thursday, April 07, 2011 Sheet 25 of 109

5

4

3

2

1

D

D

C

C

B

B

A

A

WWW.ALISALER.COM

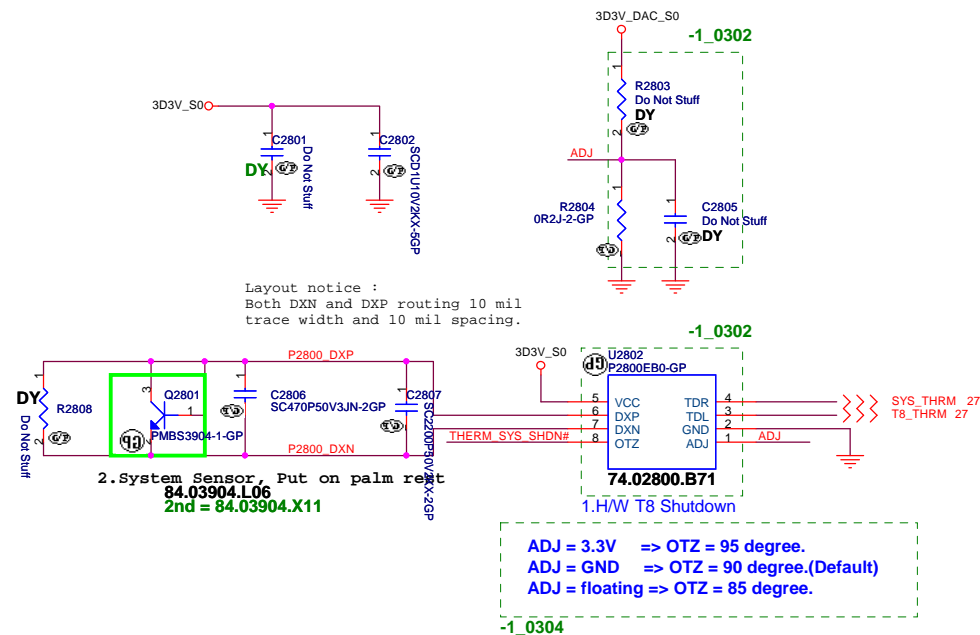
D12G

<div><div>緯創資通</div><div>Wistron Corporation</div><div>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</div></div>		
Title <div>Clock(colay)</div>		
Size <div>A4</div>	Document Number <div>BA40-HR</div>	Rev <div>SD</div>
Date <div>Thursday, April 07, 2011</div>		Sheet <div>26</div> of <div>109</div>

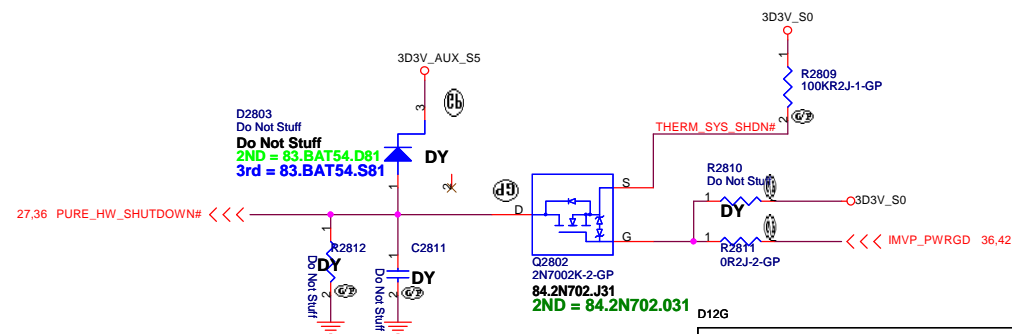
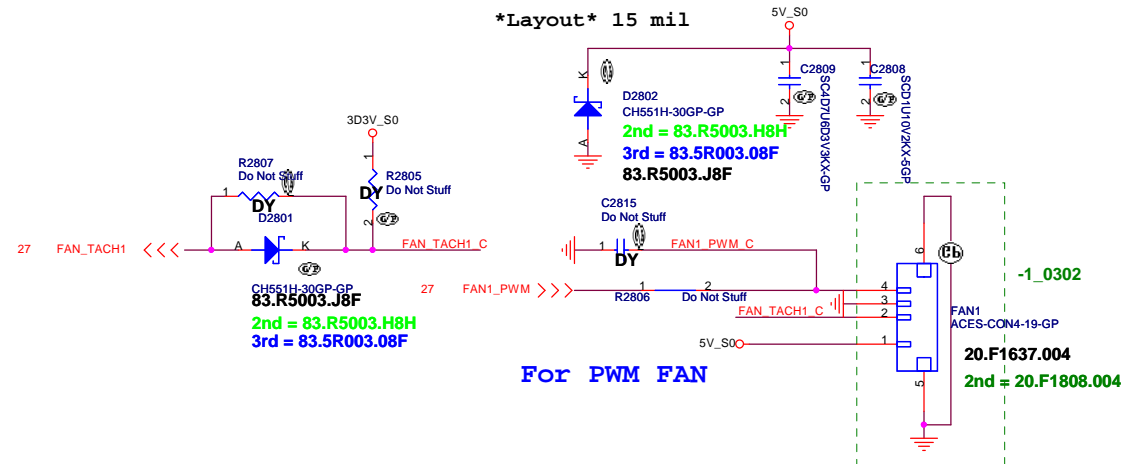


SSID = Thermal

Thermal sensor P2800



Fan controller P2793



緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title		
Thermal P2800/Fan Controller P2793		
Size	Document Number	Rev
Custom	BA40-HR	SD
Date: Thursday, April 07, 2011 Sheet 28 of 109		



AUDIO OP AMPLIFIER

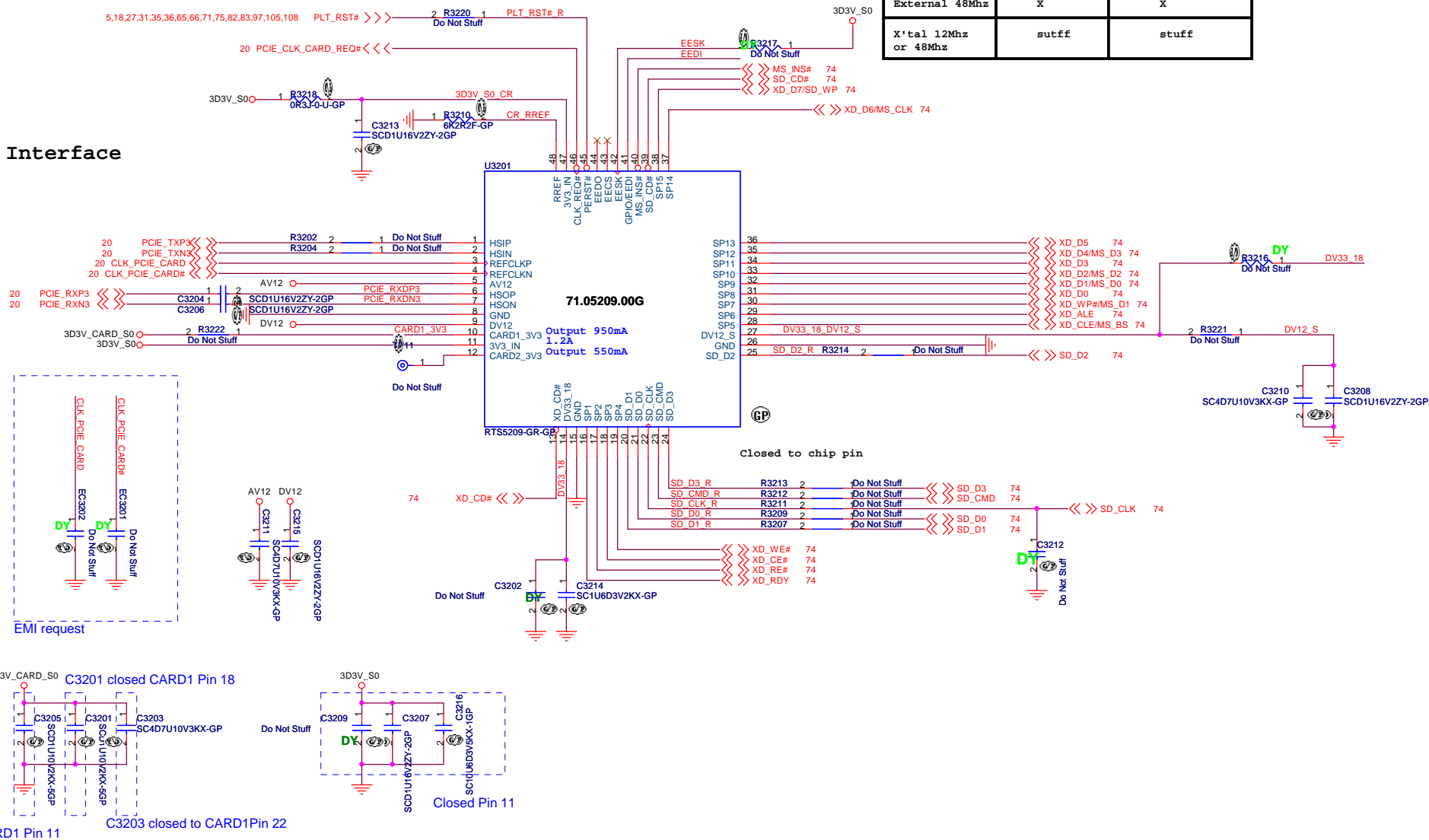
JE40 delete AMP function

WWW.ALISALER.COM

D12G

		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
Audio AMP			
Size A4	Document Number BA40-HR		Rev SD
Date: Thursday, April 07, 2011		Sheet 30 of	109

RTS5209==>PCI-E Interface



WWW.ALISALER.COM

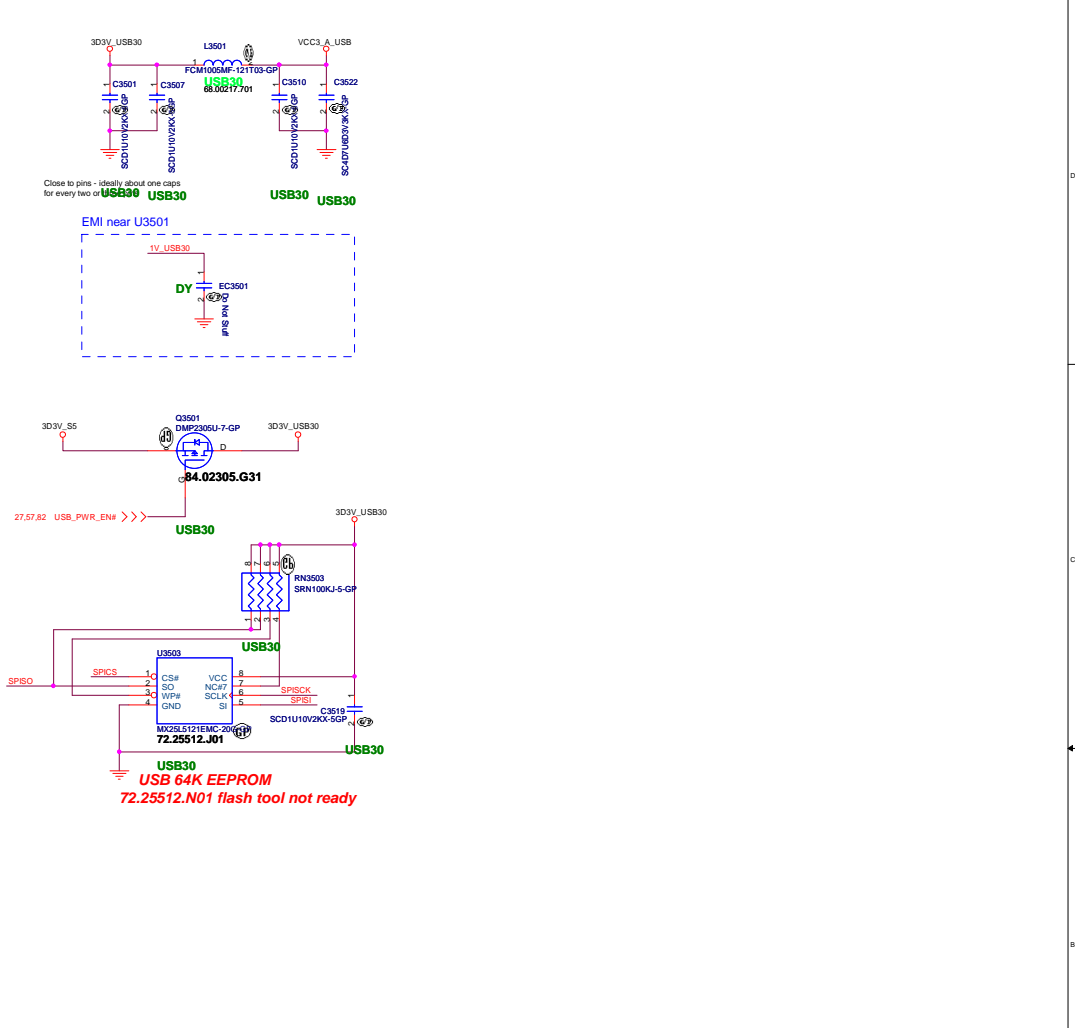
(Blanking)

D12G

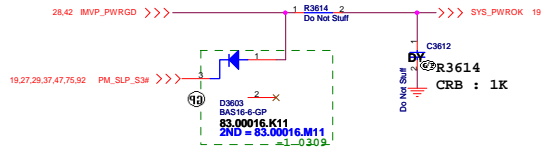
<div>緯創資通</div> <div>Wistron Corporation</div> <div>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</div>		
Title <div>Reserved</div>		
Size <div>A4</div>	Document Number <div>BA40-HR</div>	Rev <div>SD</div>
Date: Thursday, April 07, 2011		Sheet 33 of 109

D12G

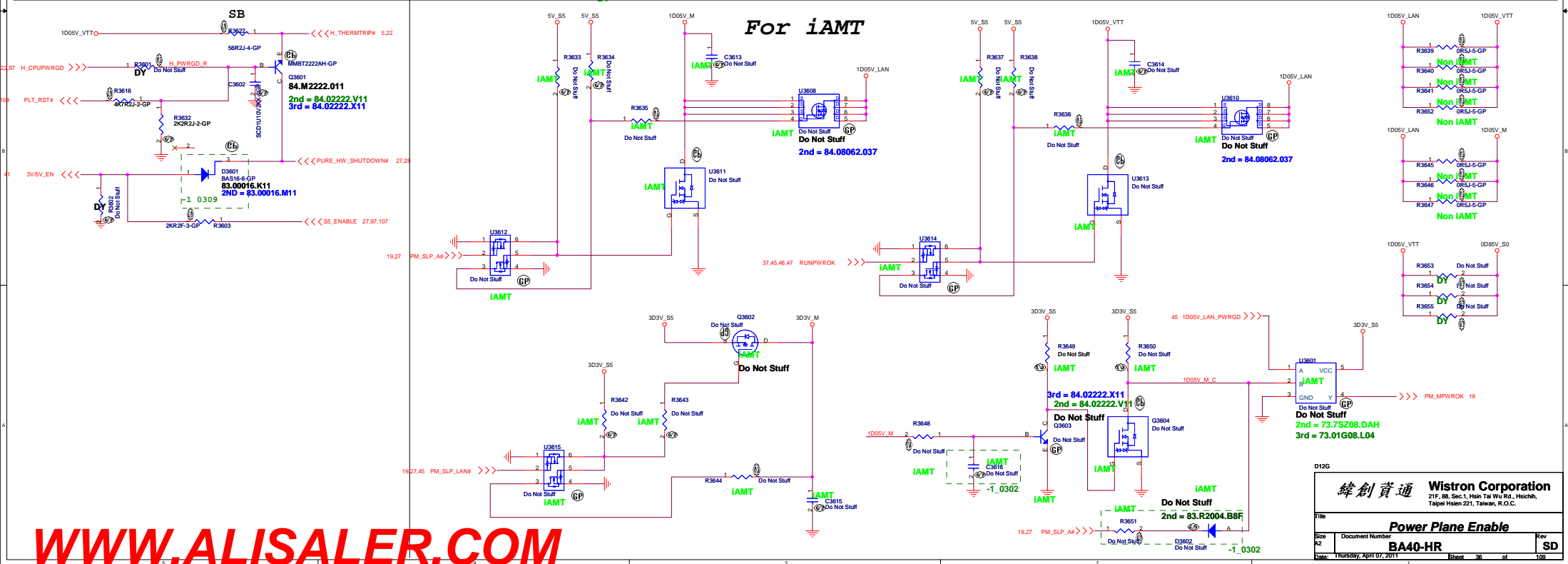
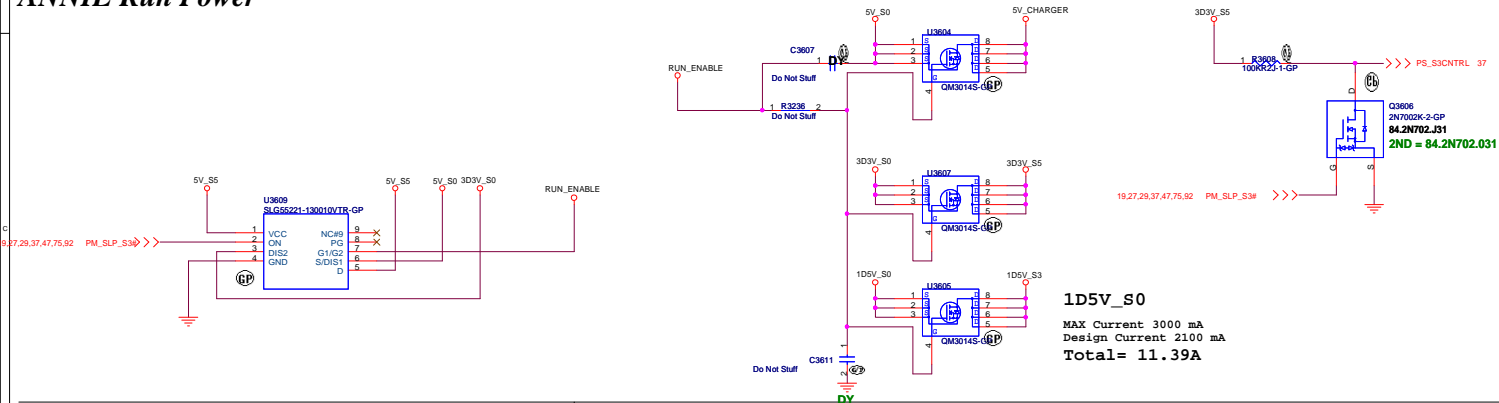
<div>緯創資通</div>		<div>Wistron Corporation</div>	
		<div>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</div>	
Title			
Reserved			
Size	Document Number		Rev
A3	BA40-HR		SD
Date:	Thursday, April 07, 2011		Sheet 34 of 109



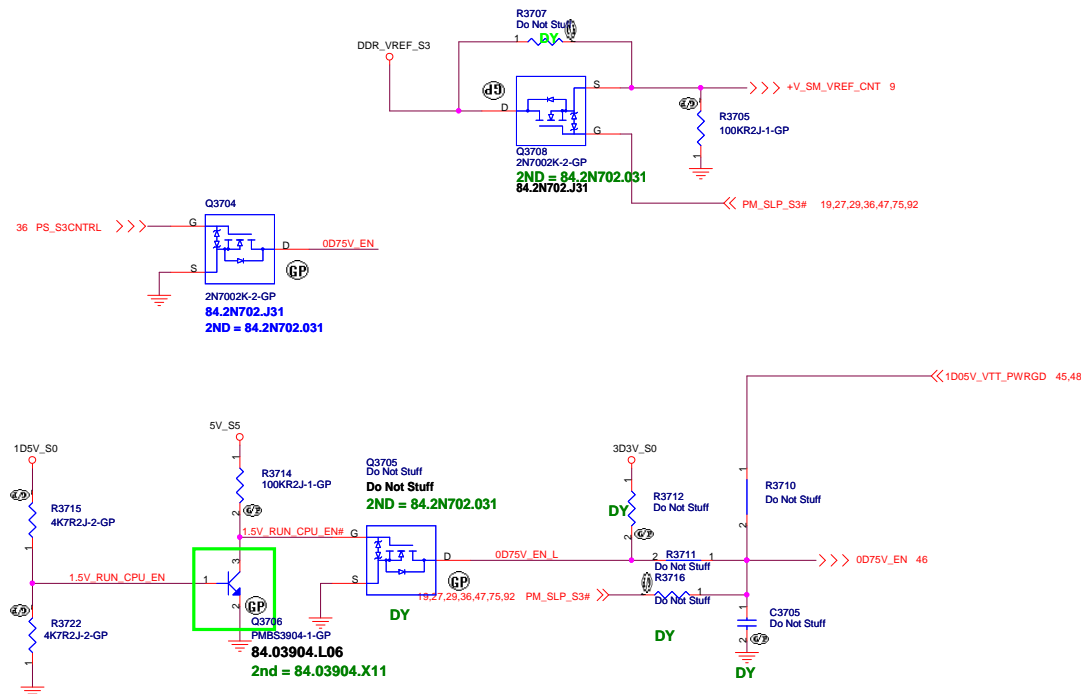
Power Sequence



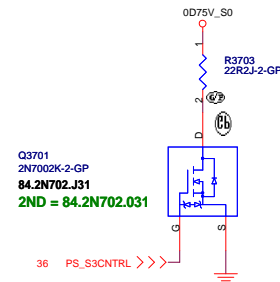
ANNIE Run Power



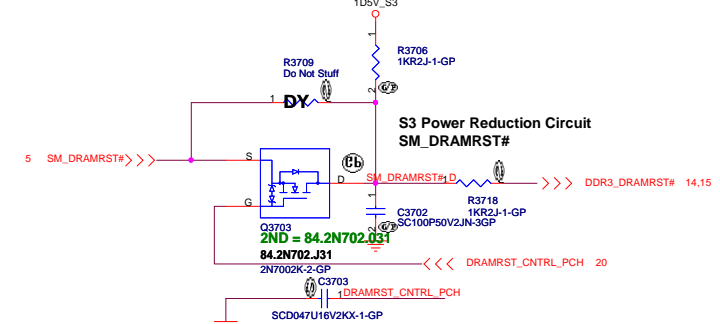
Close to CPU
S3 Power Reduction Circuit Processor VREF_DQ Implementation



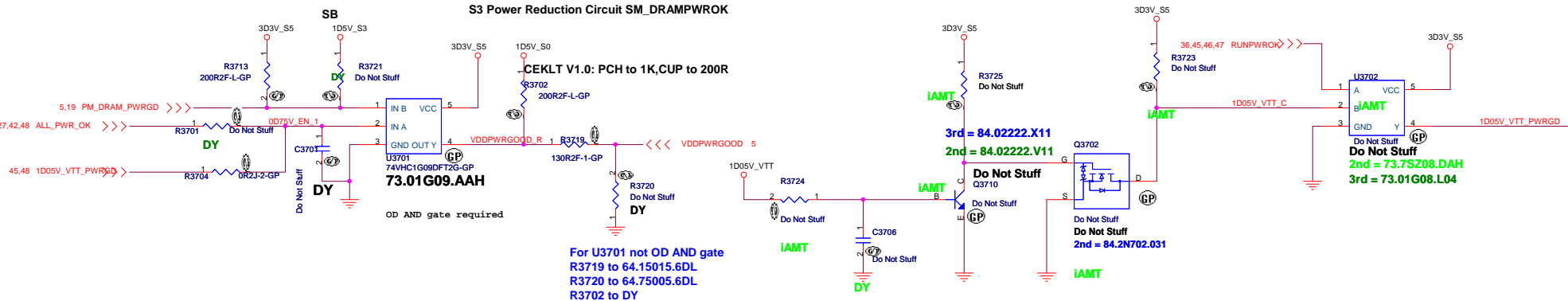
Close to DIMM
S3 Power Reduction Circuit SM_DRAMPWROK



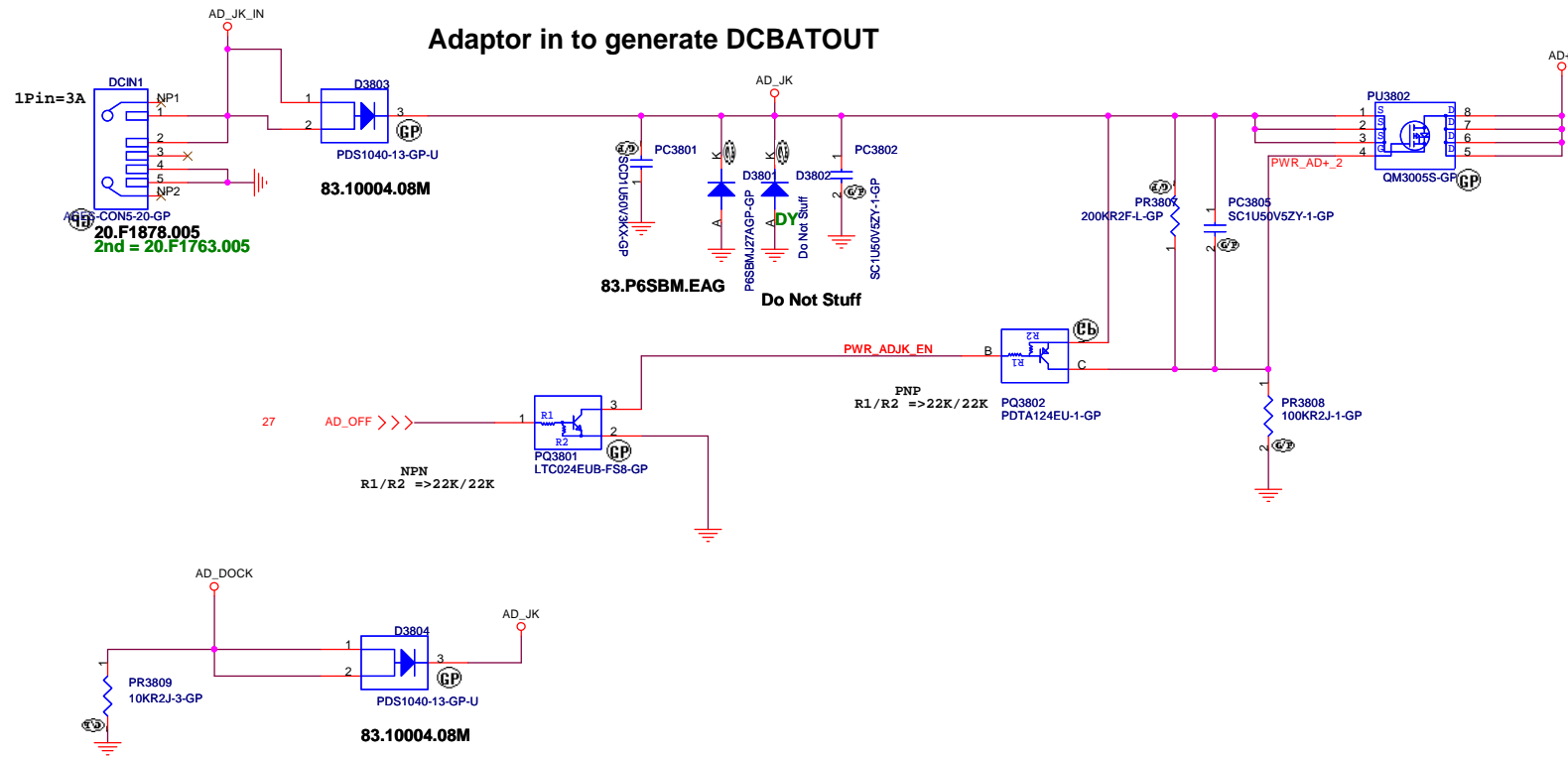
Close to CPU
S3 Power Reduction Circuit SM_DRAMPWROK



Close to CPU
S3 Power Reduction Circuit SM_DRAMPWROK



SM_DRAMPWROK must have a maximum of 15ns rise or fall time over $VDDQ \pm 0.55 \pm 200\text{mV}$ and the edge must be monotonic

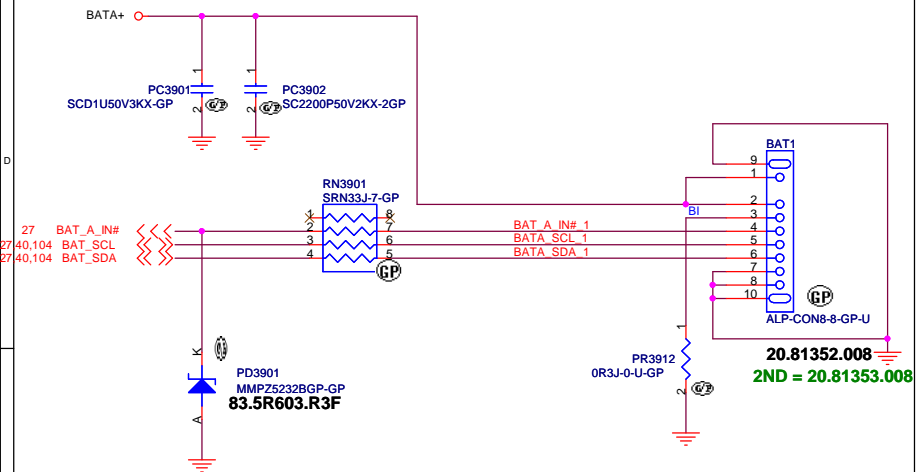


D12G

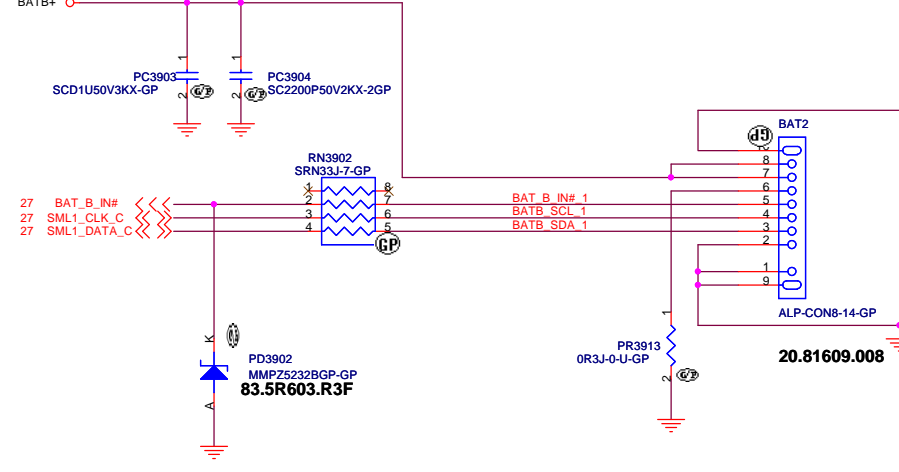
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title			DCIN JACK
Size	Document Number	Rev	
A3	BA40/50-HR	SD	
Date:	Thursday, April 07, 2011	Sheet	38 of 109

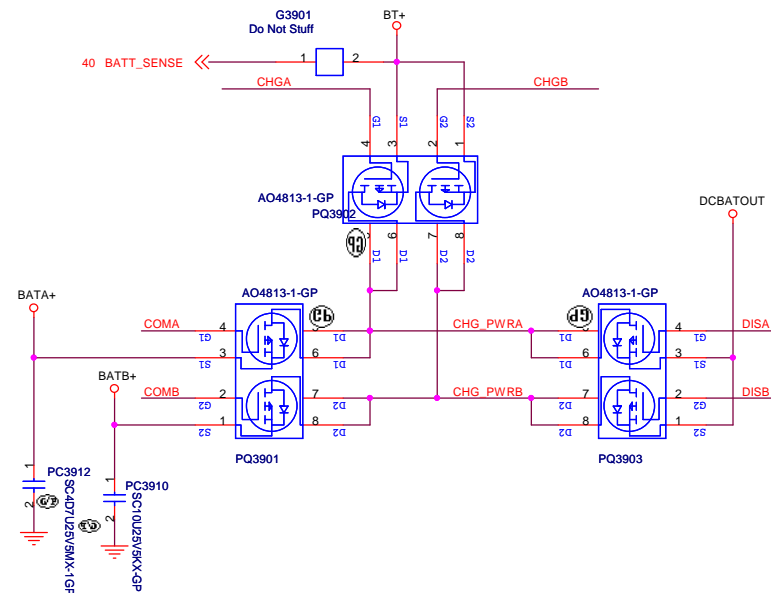
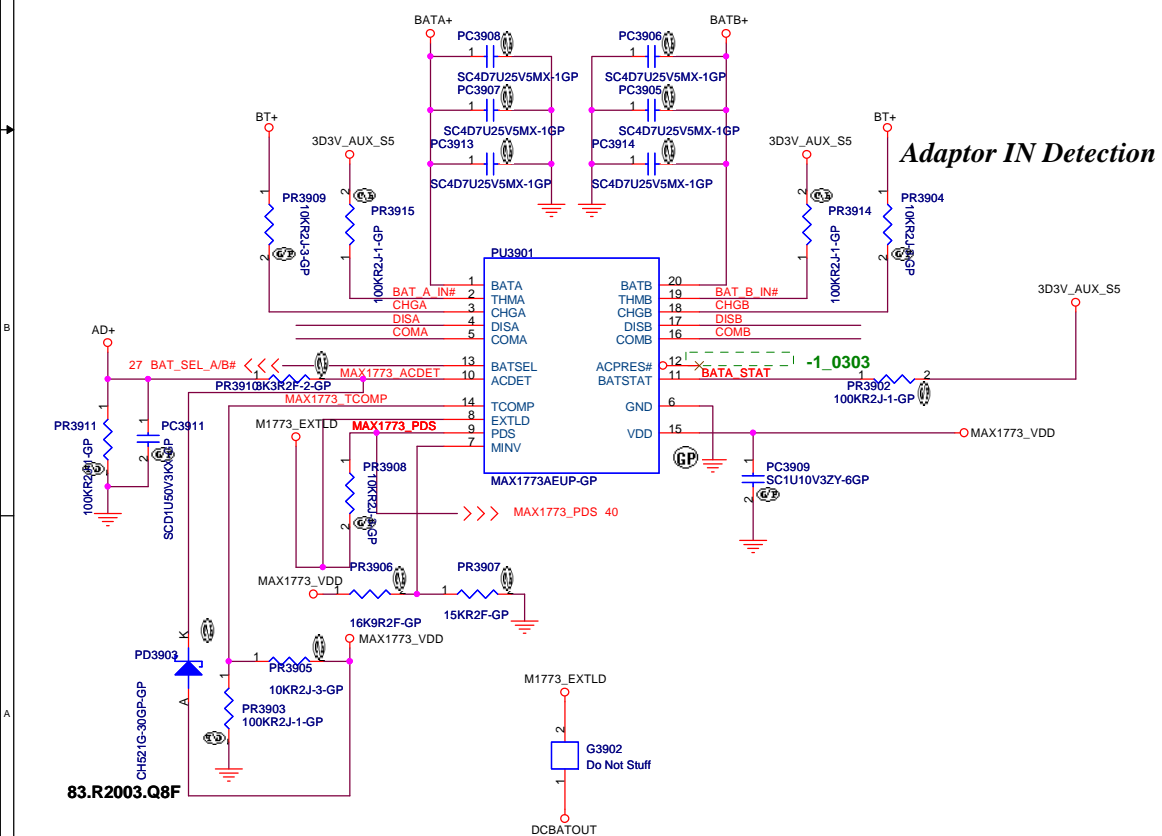
MAIN BATTERY CONNECTOR



2nd BATTERY CONNECTOR



BATTERY SWITCH



D12G

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

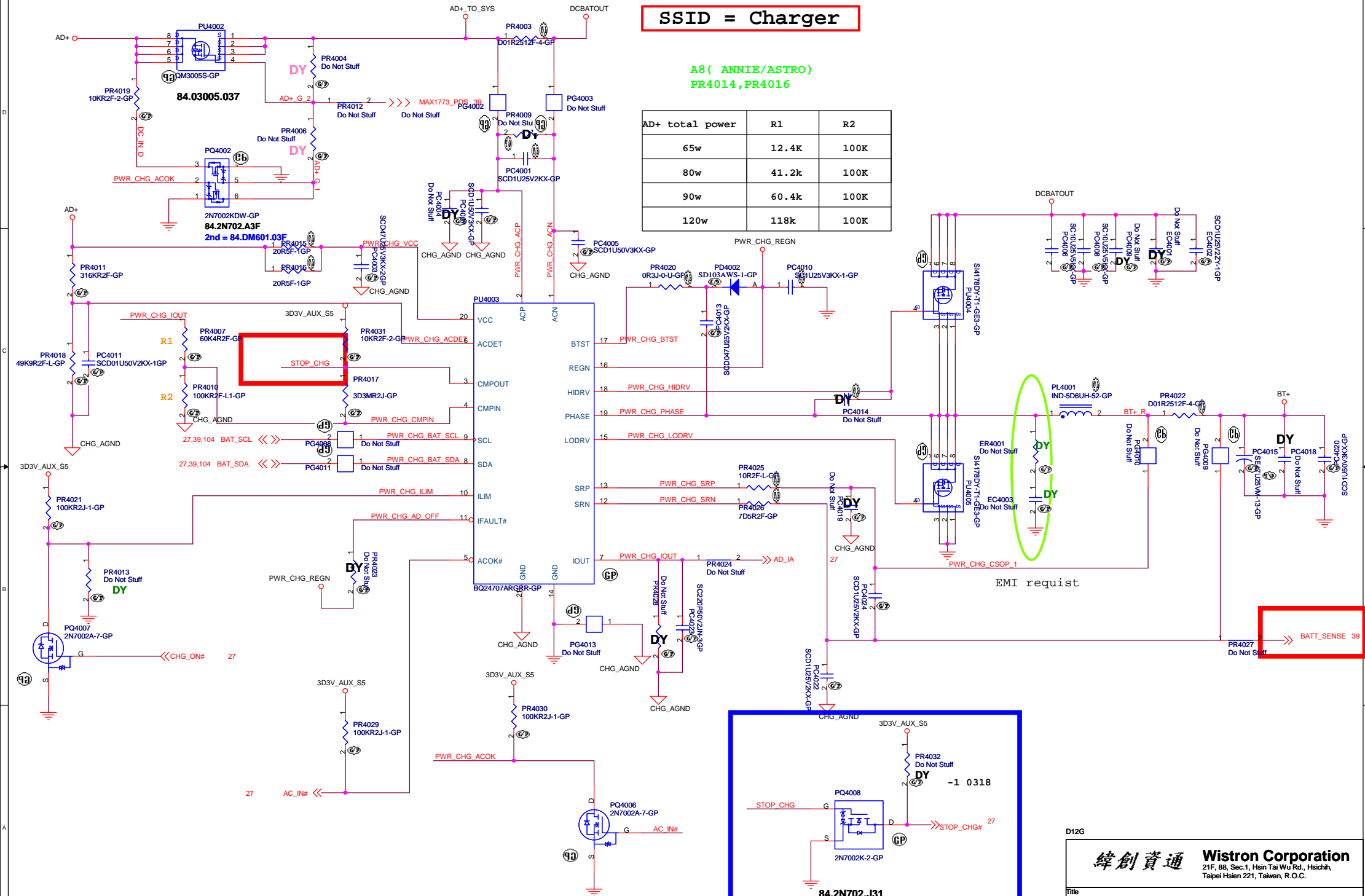
Title			
BATT CONN			
Size A3	Document Number		Rev
	BA40/50-HR		SD
Date:	Thursday, April 07, 2011	Sheet 39 of	109

WWW.ALISALER.COM

SSID = Charger

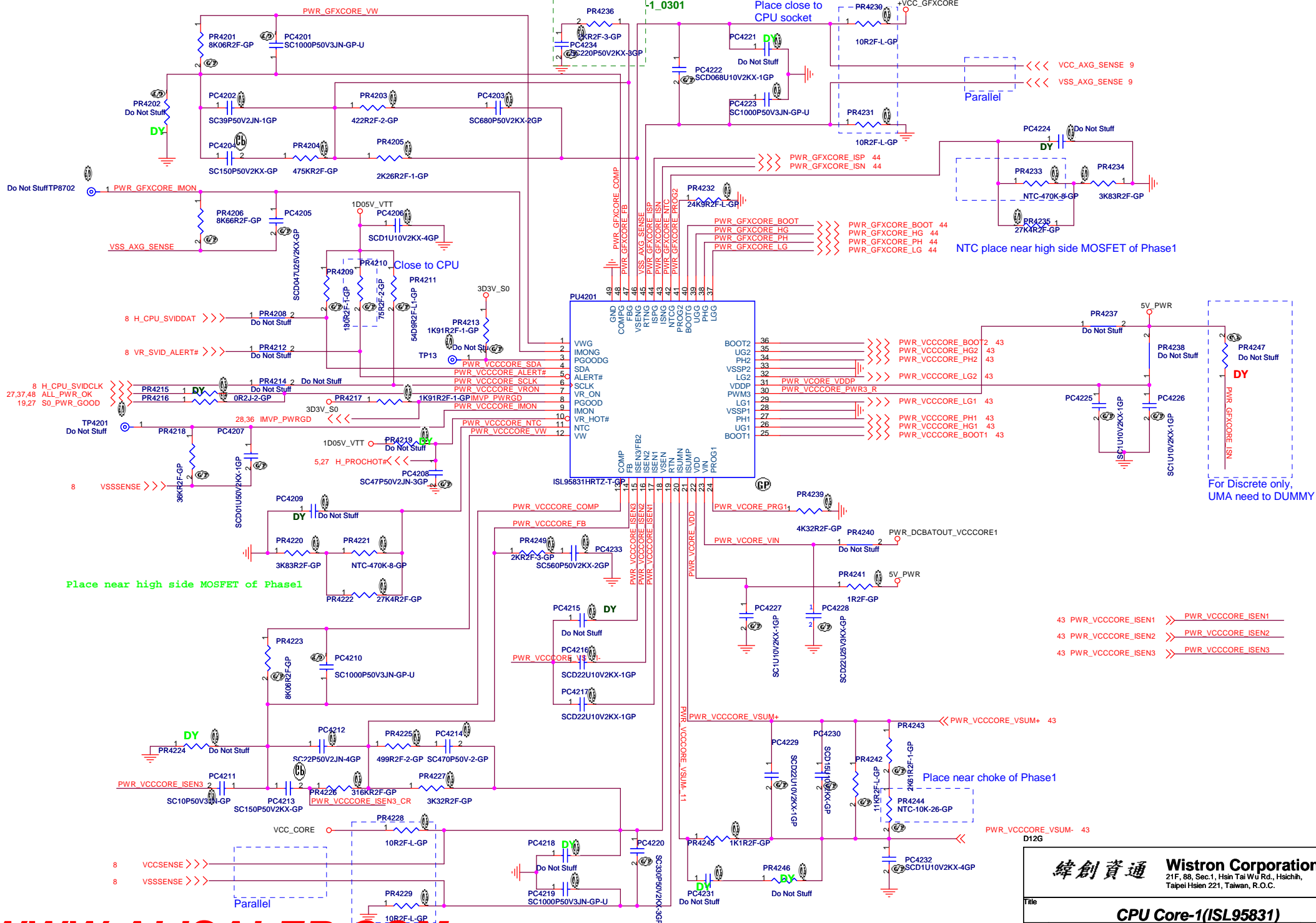
A8(ANNIE/ASTRO)
PR4014,PR4016

AD+ total power	R1	R2
65w	12.4K	100K
80w	41.2k	100K
90w	60.4k	100K
120w	118k	100K

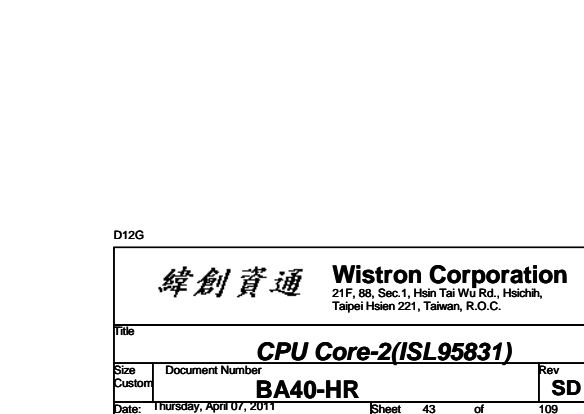
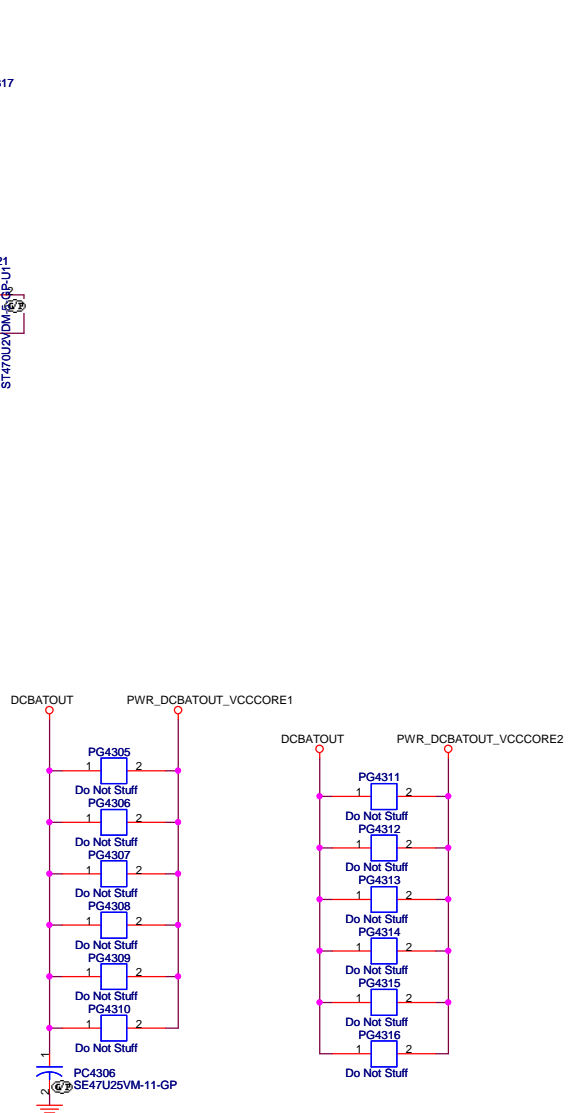
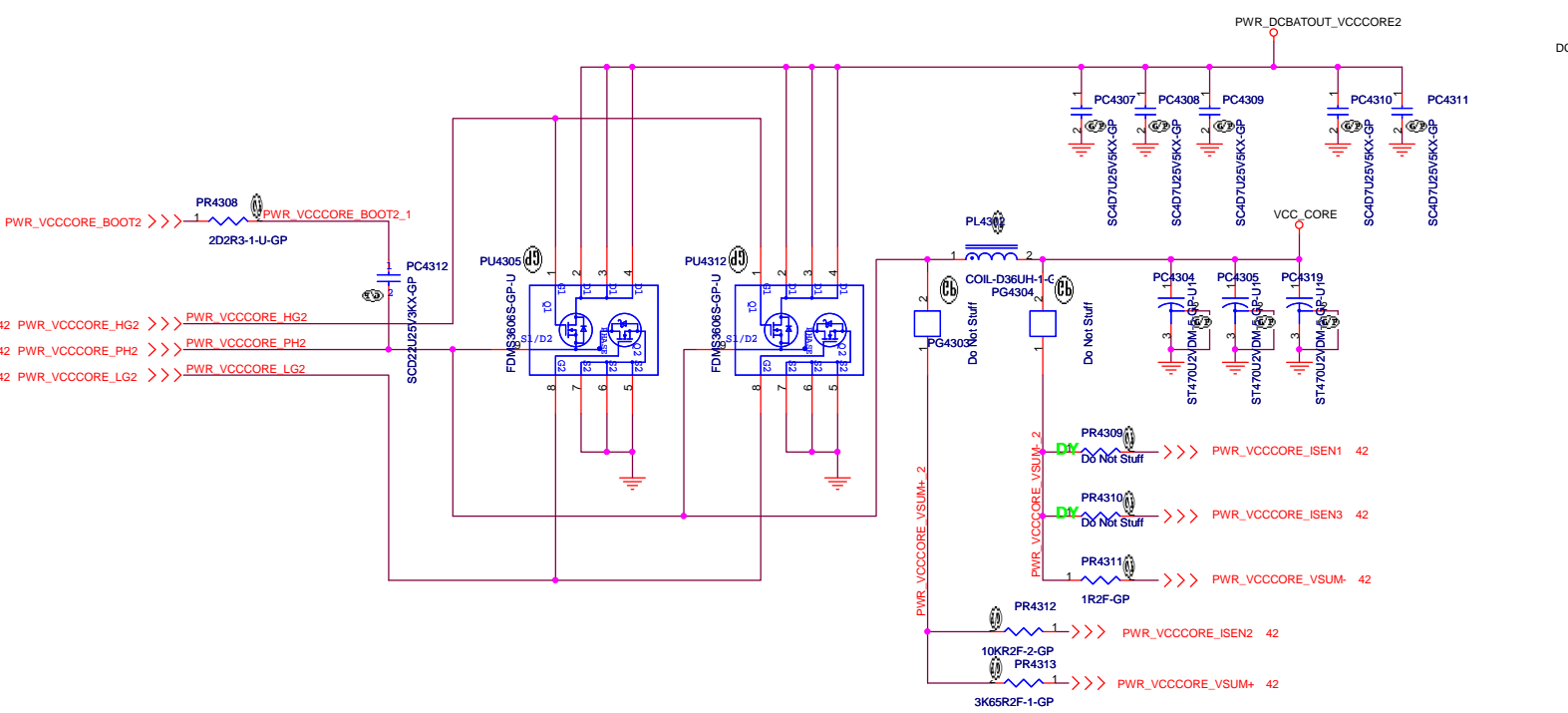
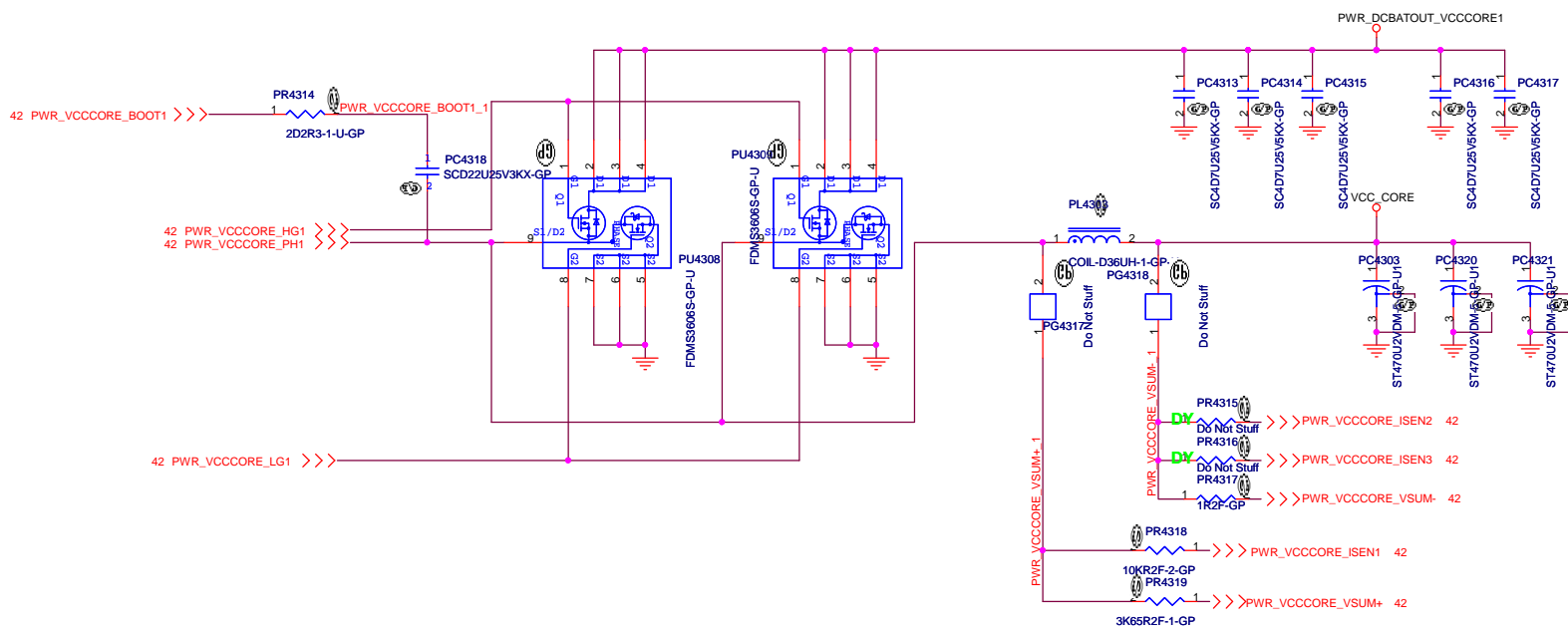


WWW.ALISALER.COM

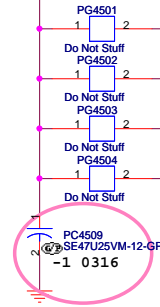




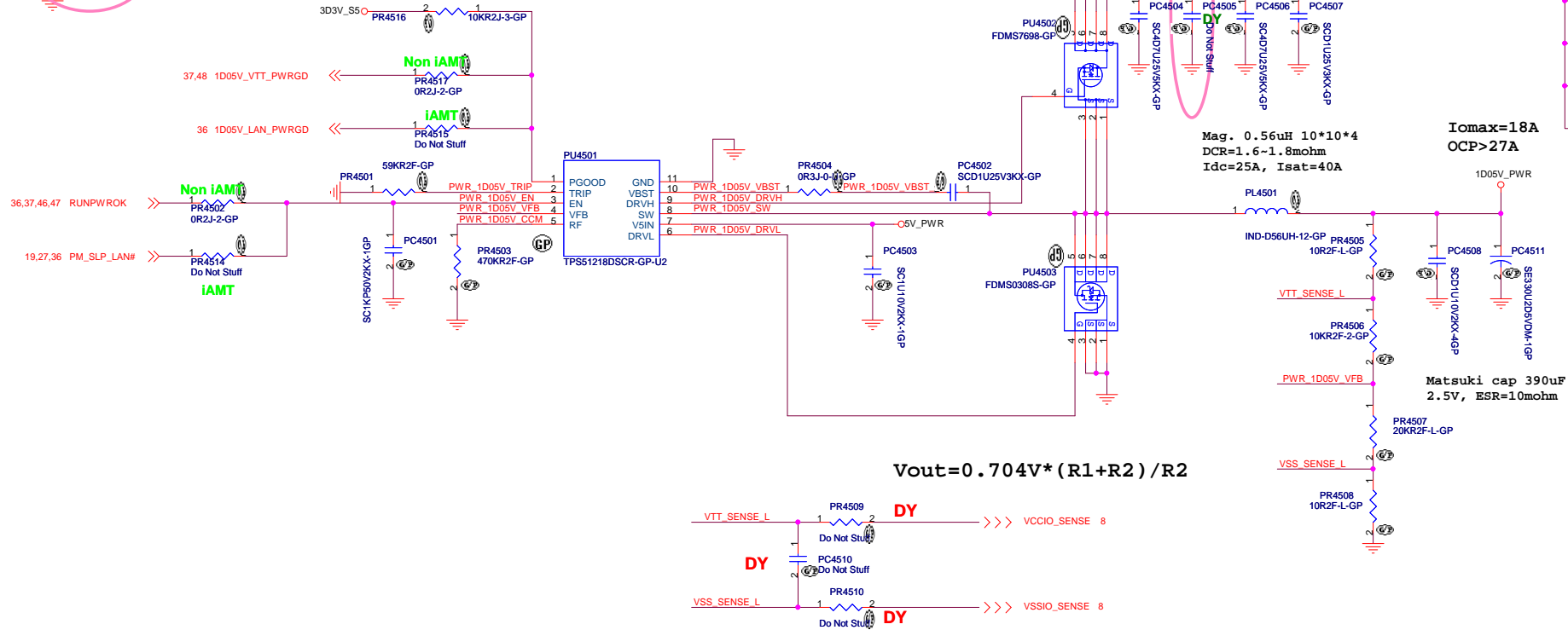
WWW.ALISALER.COM



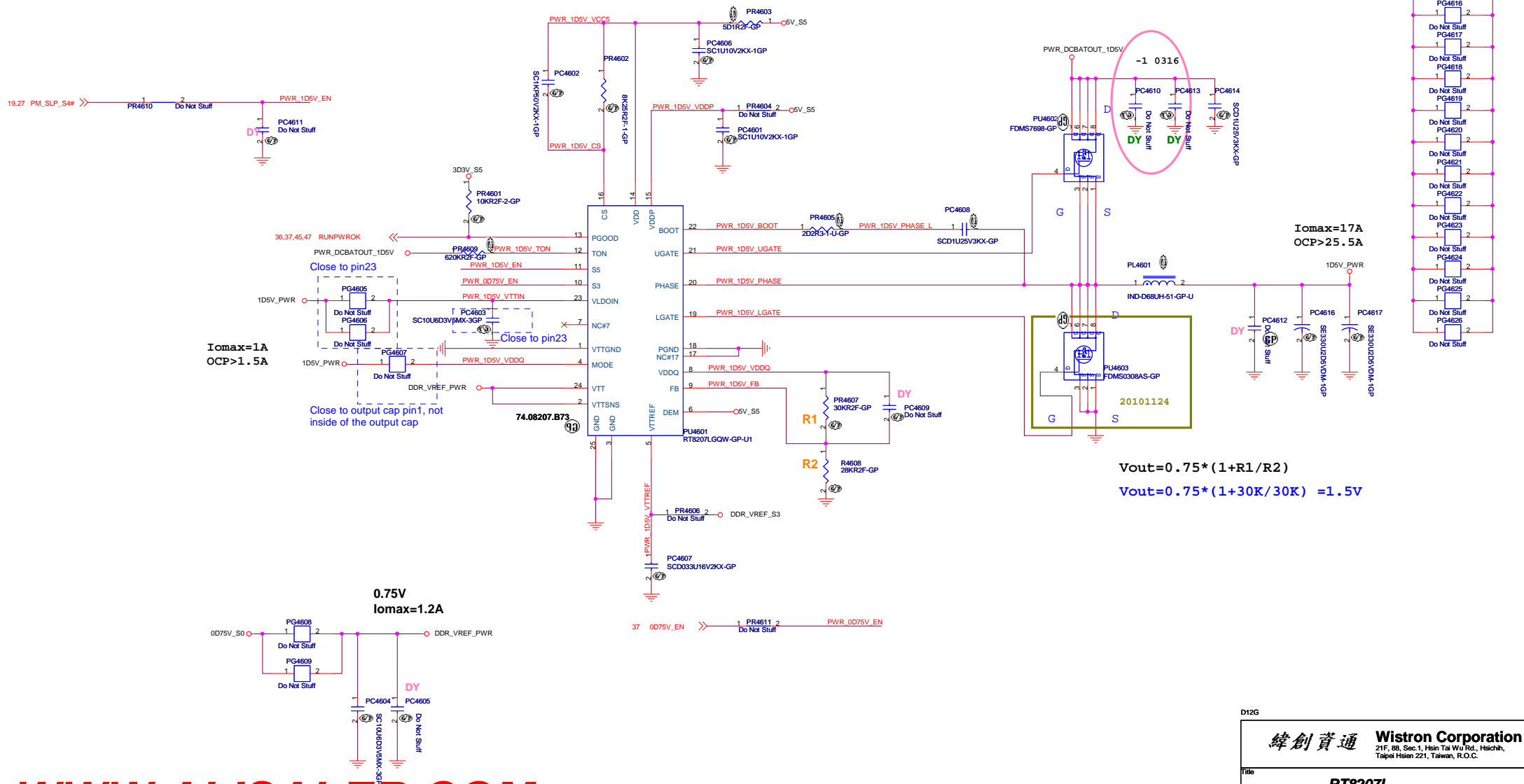
DCBATOUT PWR_DCBATOUT_1D05V



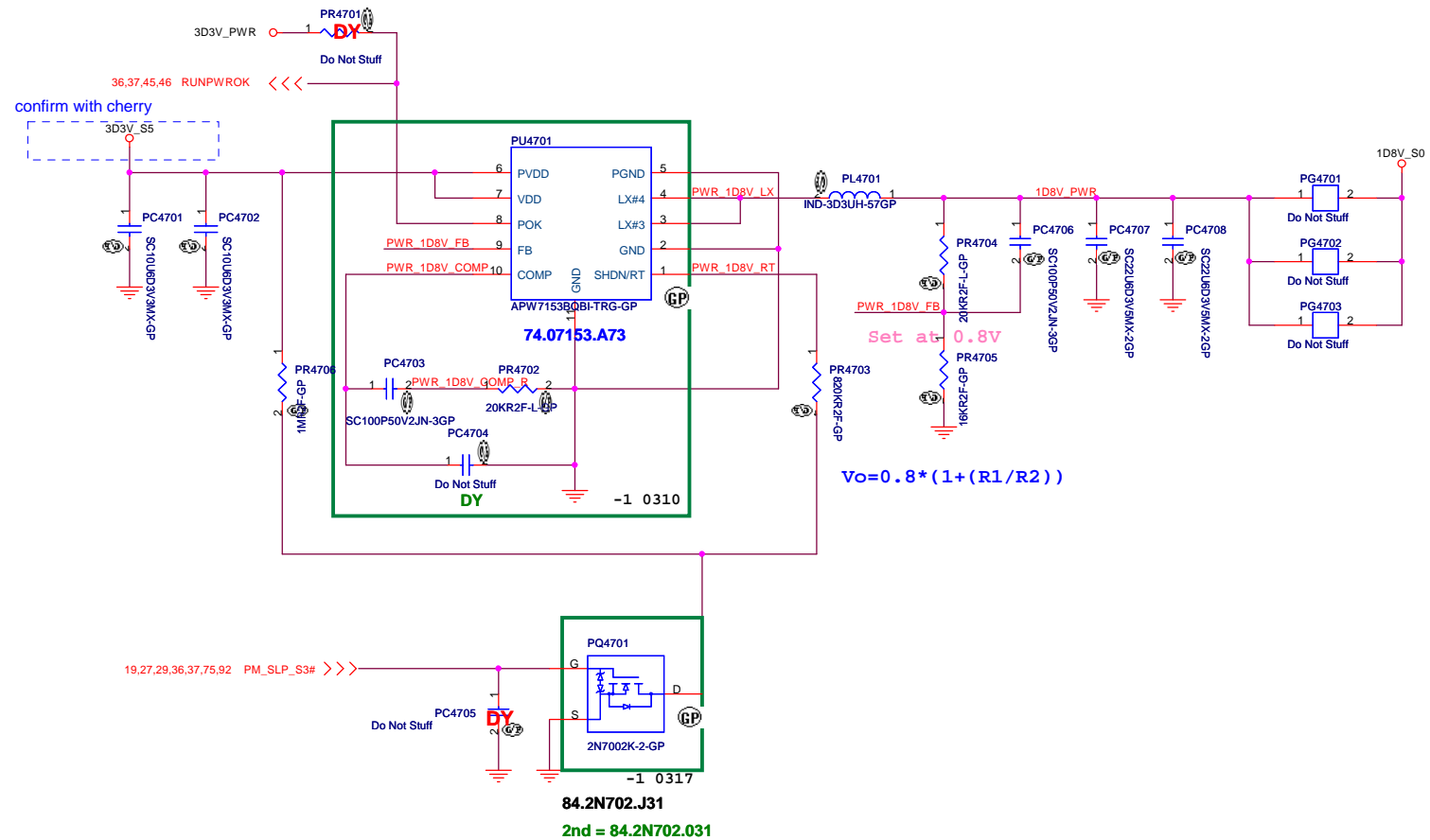
TPS51218 for 1D05V



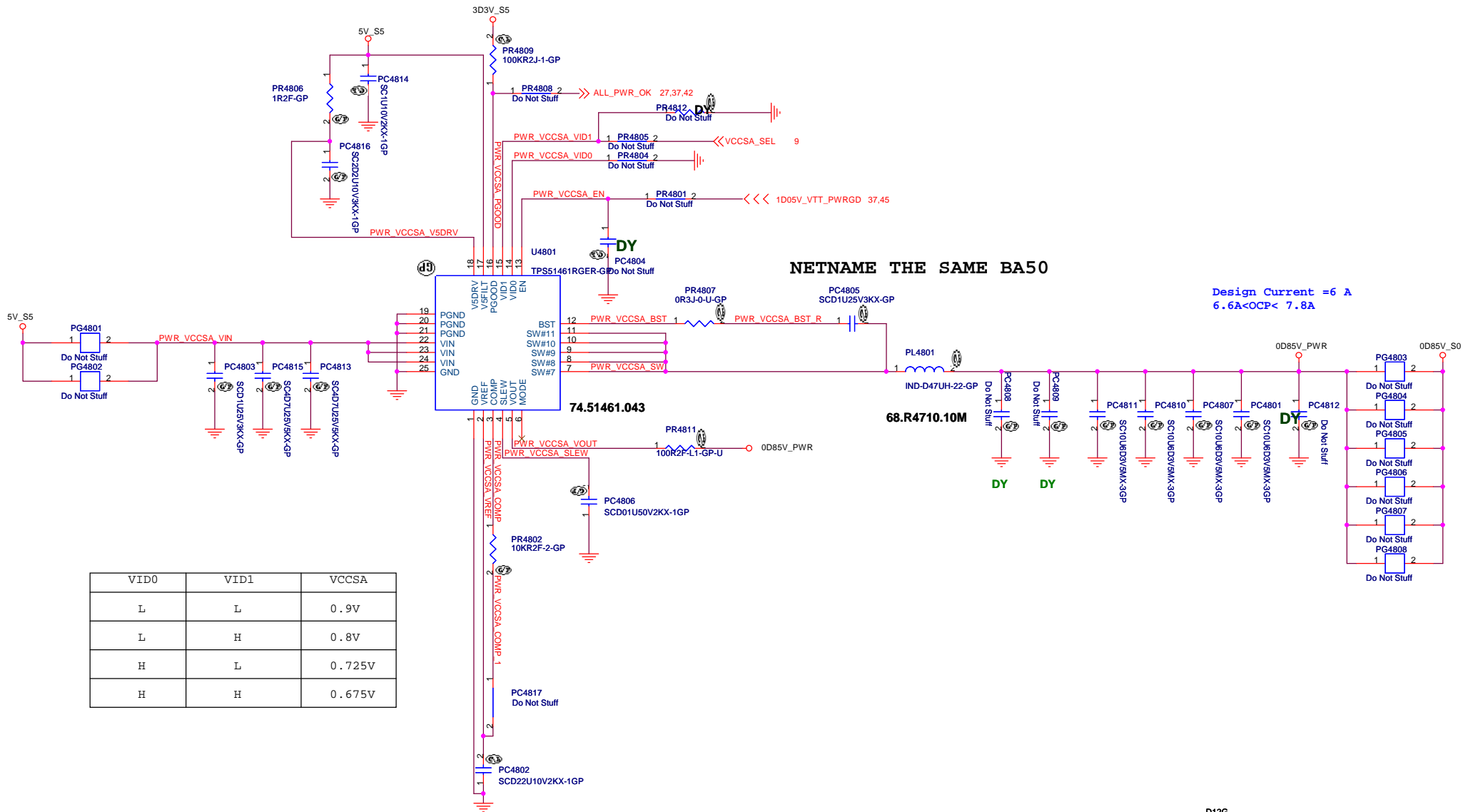
RT8207L for 1D5V



RT8015B for 1D8V_S0



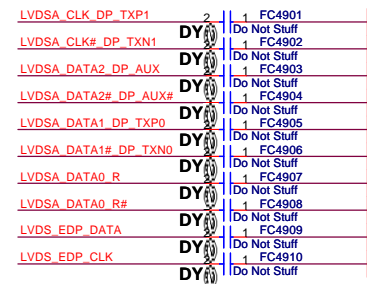
TPS51461 for VCCSA



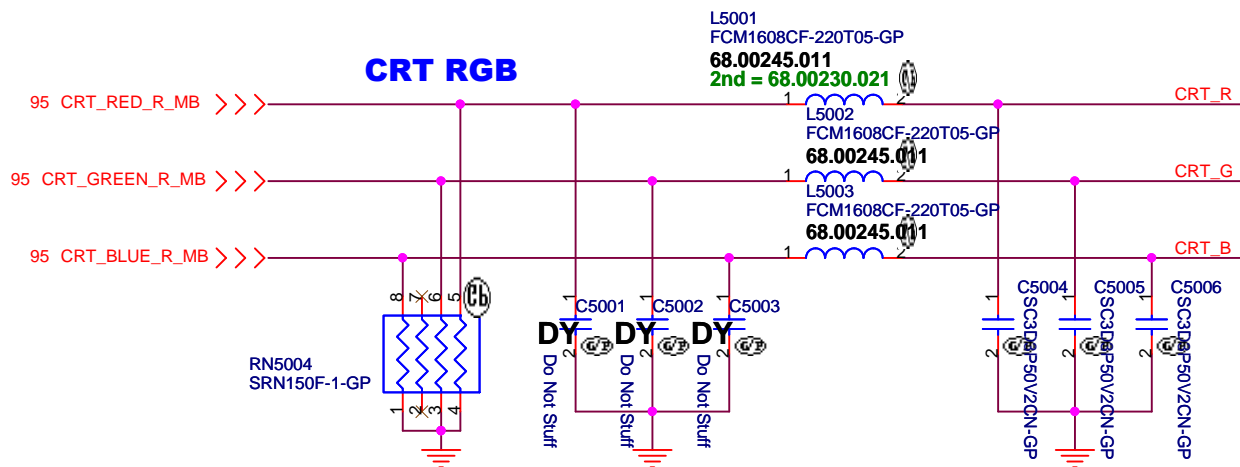
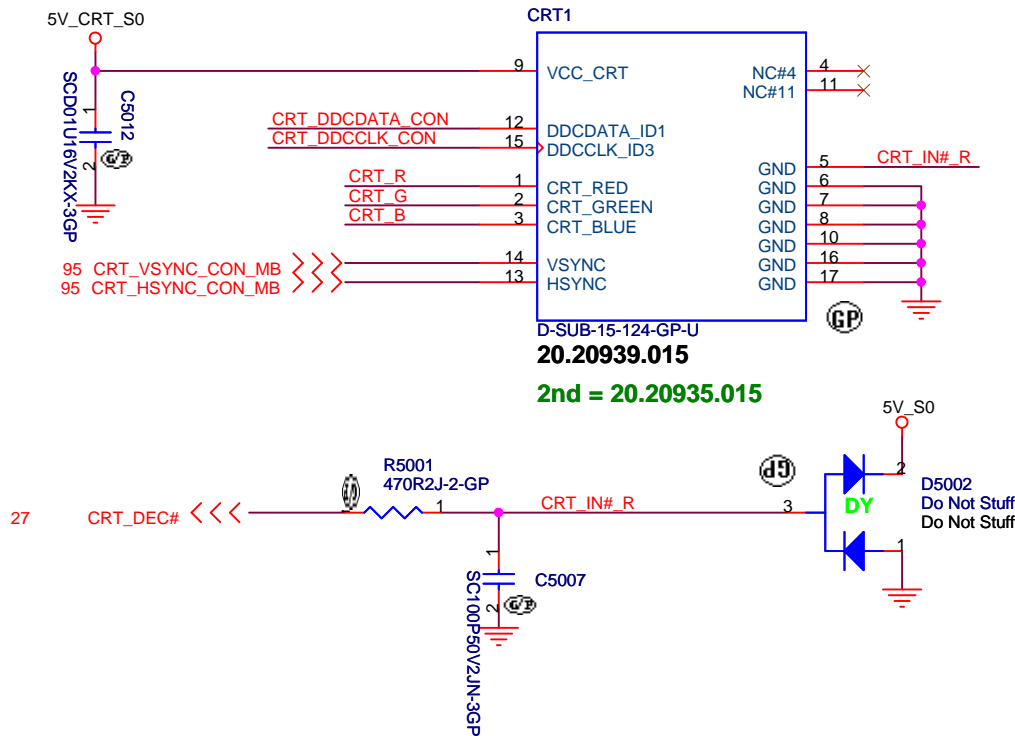
NETNAME THE SAME BA50

Design Current =6 A
6.6A<OCP< 7.8A

INVERTER POWER

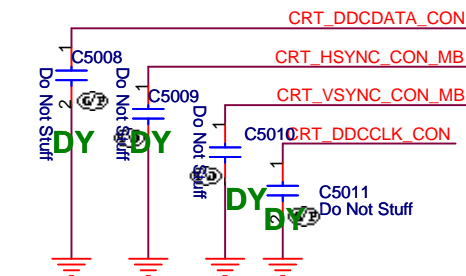
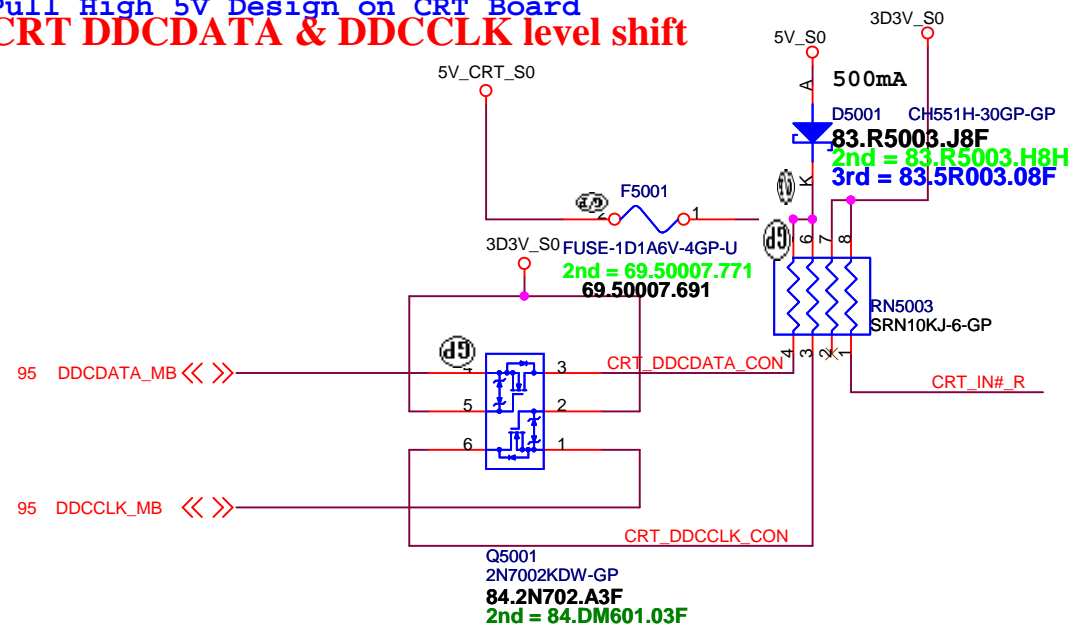


Title			
LCD Connector			
Size A3	Document Number		Rev
	BA40-HR		SD
Date:	Thursday, April 07, 2011	Sheet 49 of	109



0806 check RN5004 擺放位置

Pull High 5V Design on CRT Board CRT DDCDATA & DDCCLK level shift

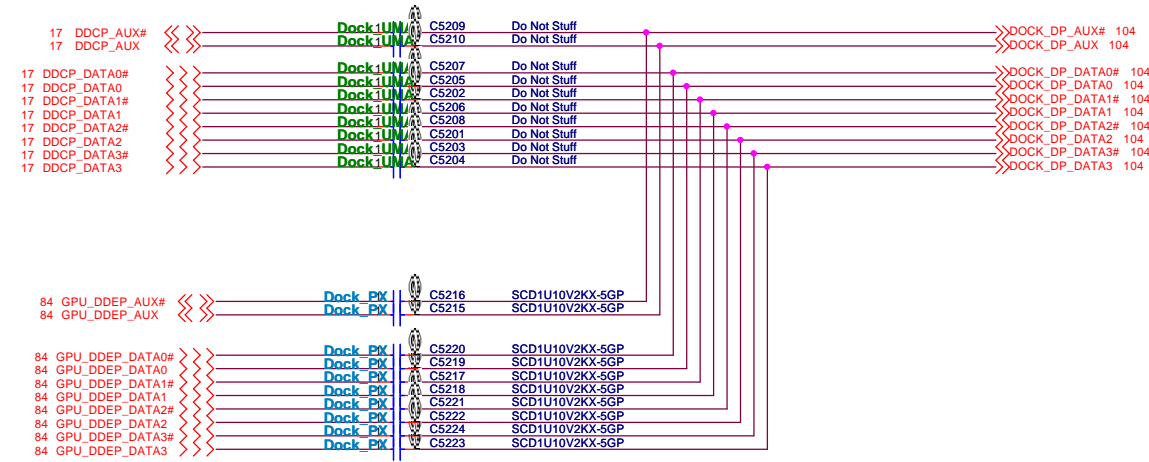
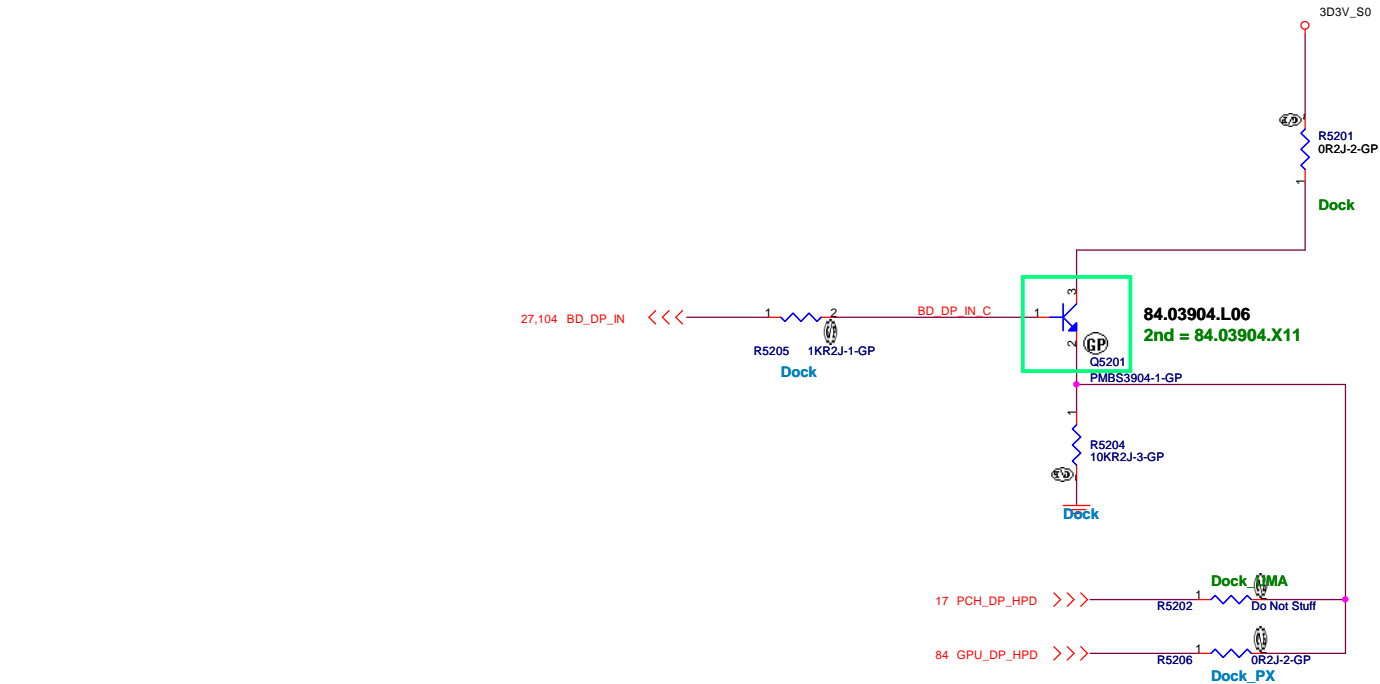


D12G

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title		
CRT Connector		
Size	Document Number	Rev
A4	BA40-HR	SD
Date	Thursday, April 07, 2011	Sheet 50 of 109

DP



(Blanking)

D12G

<div>緯創資通</div>		<div>Wistron Corporation</div>	
		<div>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</div>	
<div>Title</div> <div>S-VIDEO</div>			
<div>Size</div> <div>A4</div>	<div>Document Number</div> <div>BA40-HR</div>		<div>Rev</div> <div>SD</div>
<div>Date: Thursday, April 07, 2011</div>		<div>Sheet</div> <div>53</div>	<div>of</div> <div>109</div>

(Blanking)

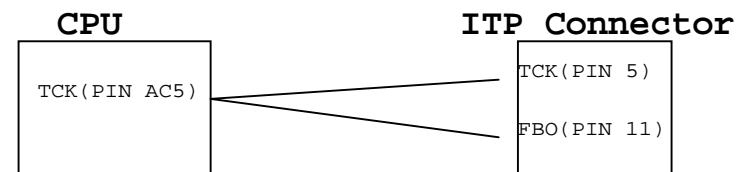
D12G

		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title Reserved			
Size A4	Document Number BA40-HR		Rev SD
Date: Thursday, April 07, 2011		Sheet 54 of	109

SSID = User.Interface

ITP Connector

H_CPURST# use pull-up Resistor close
ITP connector 500 mil (max),
others place near CPU side.



D12G

緯創資通

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

ITP

Size
A4

Document Number

BA40-HR

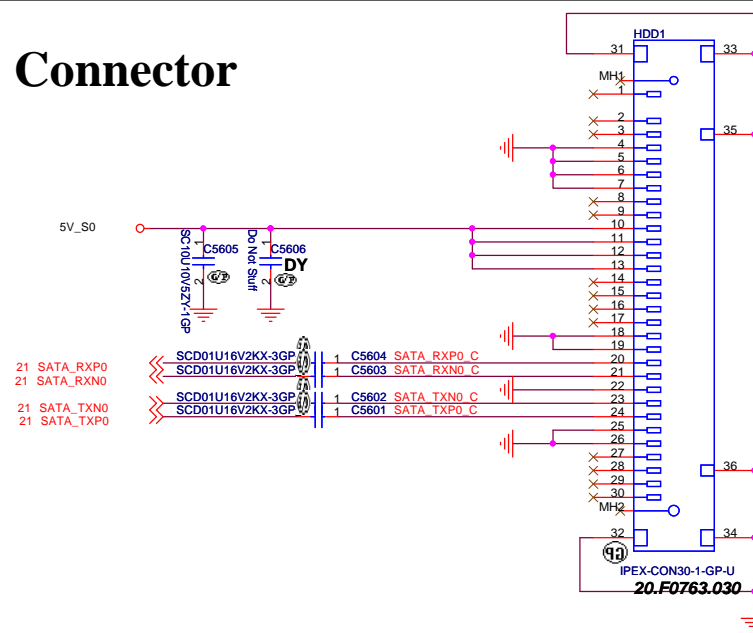
Rev
SD

Date: Thursday, April 07, 2011

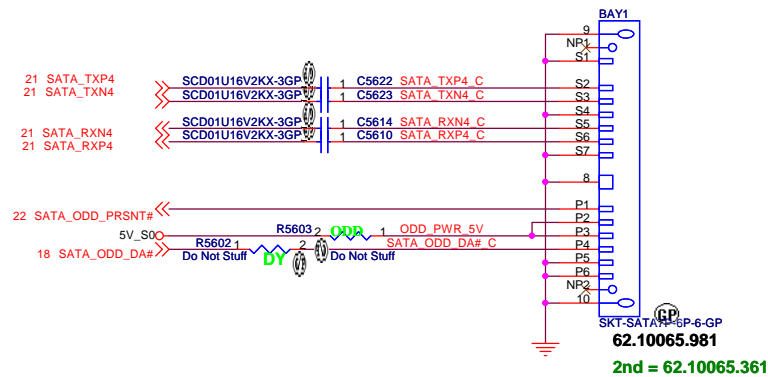
Sheet 55 of 109

SSID = SATA

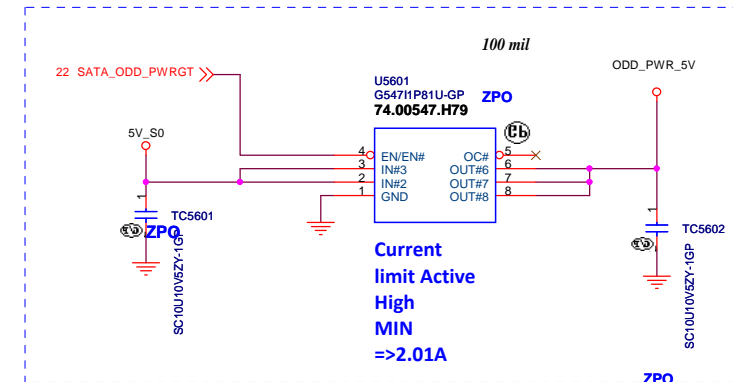
SATA HDD Connector



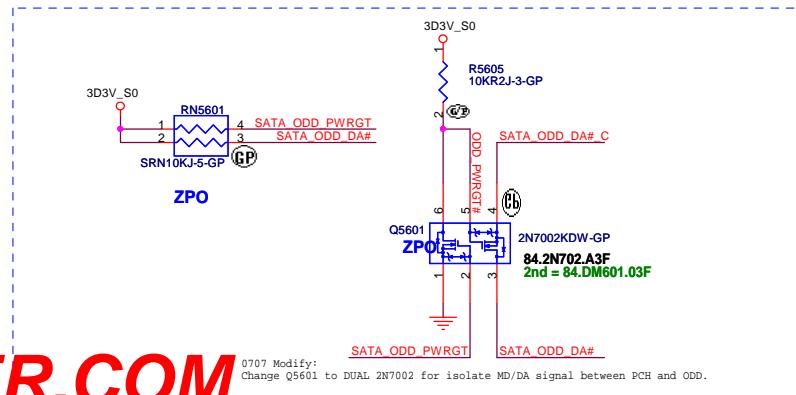
ODD Connector 2nd source 62.10065.541 and 62.10065.A11.



SATA Zero Power ODD



SATA Zero Power ODD



D12G

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
HDD/ODD	
Title	Document Number
Size A3	BA40-HR
Date: Thursday, April 07, 2011	Sheet 56 of 109

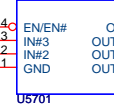
WWW.ALISALER.COM

0707 Modify:
Change Q5601 to DUAL 2N7002 for isolate MD/DA signal between PCH and ODD.

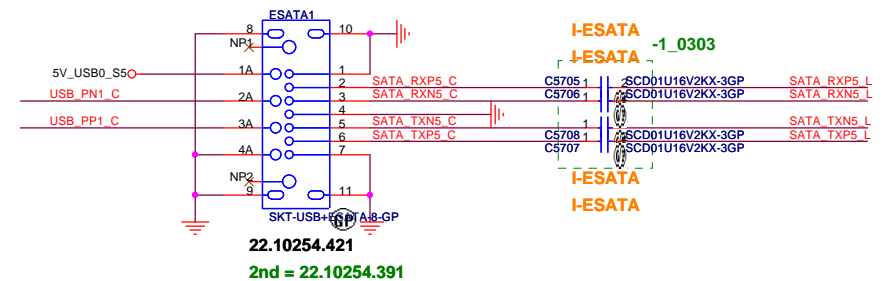
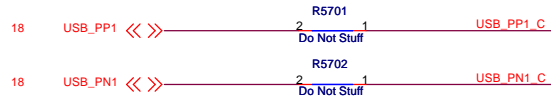
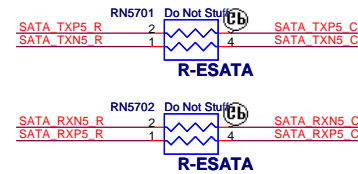
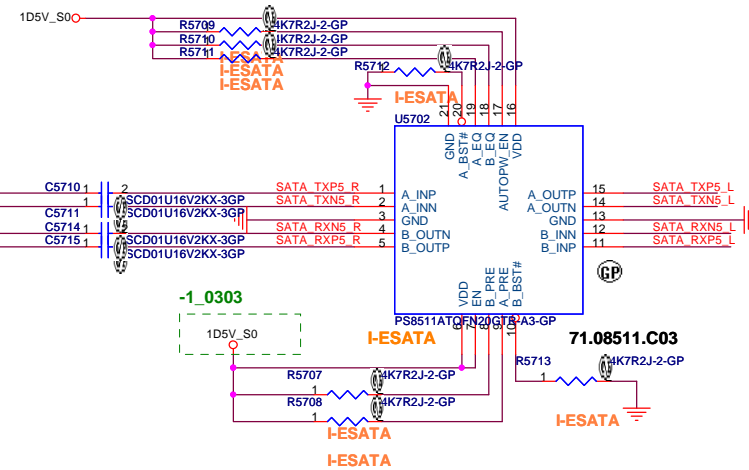
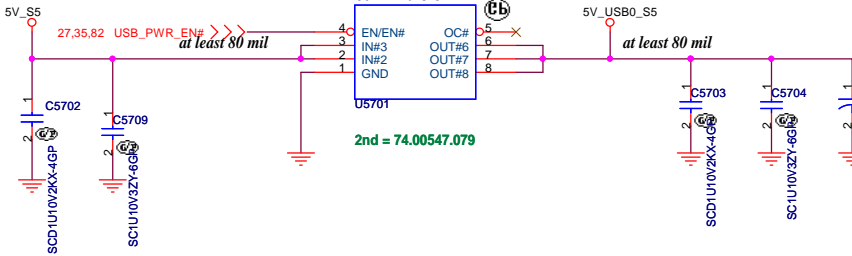
ESATA Power

MIN Current limit 2.5A
LOW ACTIVE TYPE!

G547E2P81U-GP



2nd = 74.00547.079



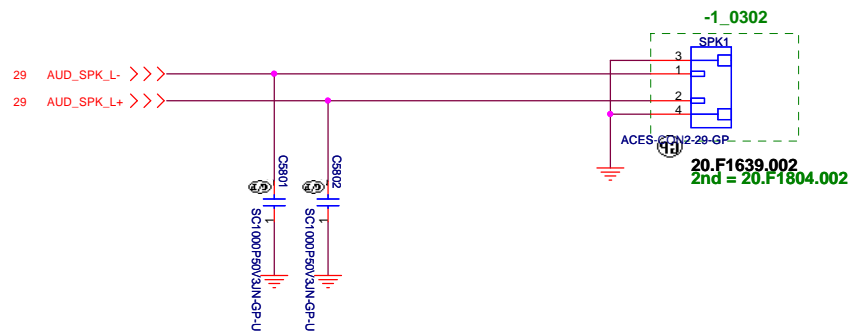
WWW.ALISALER.COM

D12G

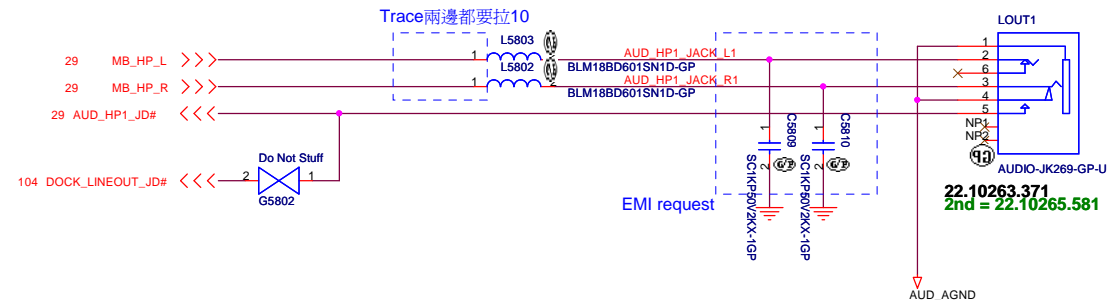
緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title E-SATA/USB CHARGER	
Size A3	Document Number BA40-HR
Date: Thursday, April 07, 2011	Sheet 57 of 109

SSID = AUDIO

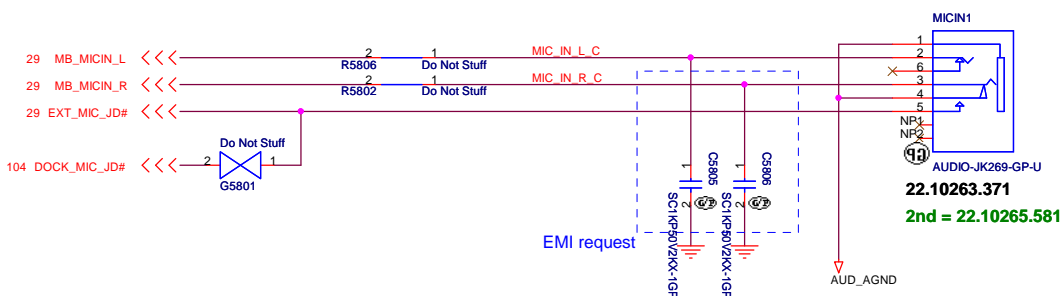
Speaker Connector



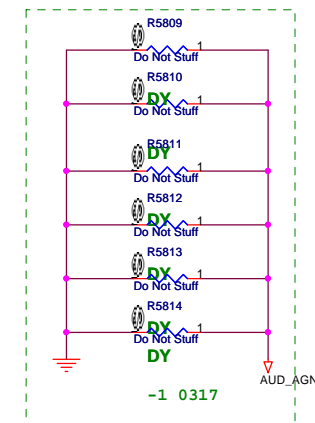
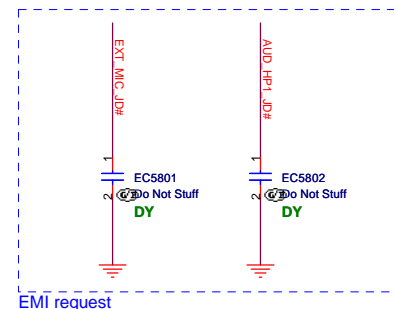
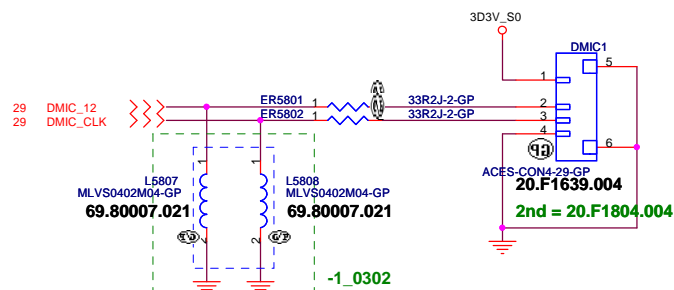
LINE1 OUT



MIC IN



Internal Microphone



WWW.ALISALER.COM

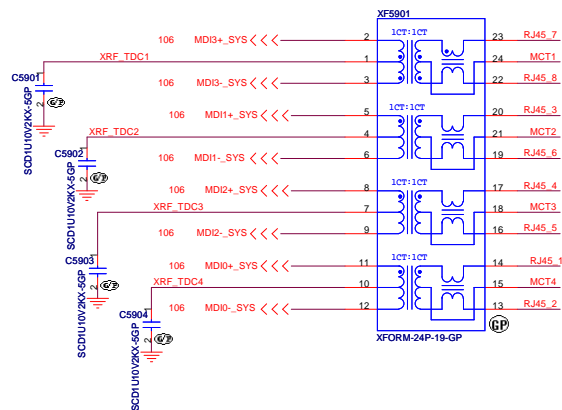
D12G

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

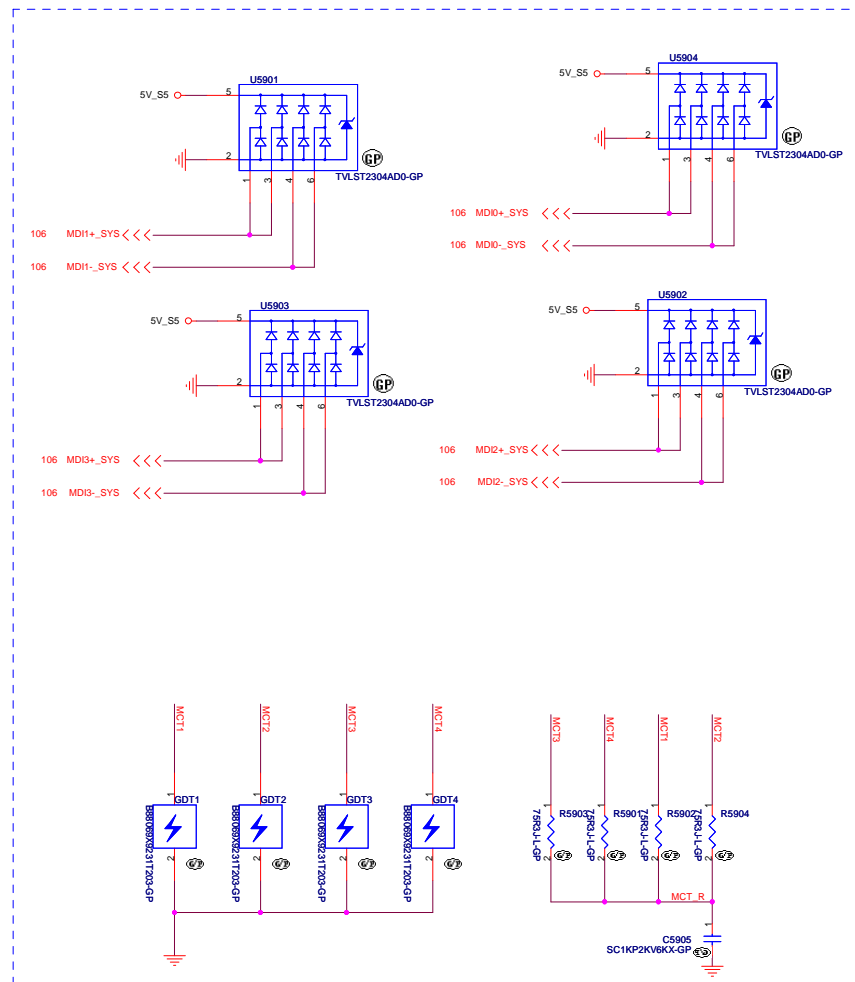
Title Audio Jack
Size A3 Document Number BA40-HR Rev SA
Date: Thursday, April 07, 2011 Sheet 58 of 109

SSID = LOM

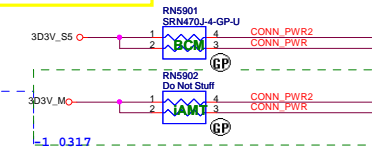
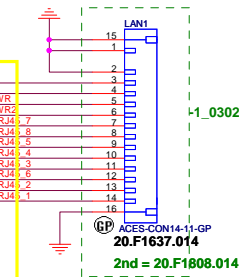
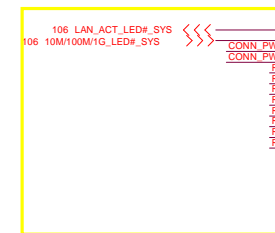
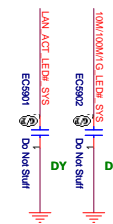
LAN MDI Off-Page



For EMI



LED COLOR

10(+): 9(-): GREEN
12(+): 13(-): ORANGE

012G

緯創資通 Wistron Corporation
21F, 88, Sec 1, Hsin Tai Wu Rd., Hsinchu,
Taipei Hsien 301, Taiwan, R.O.C.

Title: LAN CONNECTOR
Size: Document Number: BA40-HR
Date: Thursday, April 07, 2011 Sheet 59 of 109

SSID = Flash.ROM



The diagram illustrates the system architecture of the NPCE795x EC. It features three main components: a **SPI Flash** block on the left, a **Chipset** block at the top right, and the **NPCE795x EC** block at the bottom right. The **NPCE795x EC** block contains an internal **On-Chip 96K RAM** sub-block. A black line connects the **SPI Flash** to the **NPCE795x EC** block. A green line connects the **NPCE795x EC** block to the **Chipset** block, with an upward-pointing arrow labeled **Control** indicating the direction of communication.

3D3V_AUX_S5

RTC_AUX_S5

Q6001

CH715FGP-GP-U

Width=20mils

83.R0304.D81
2nd = 83.00040.E81

2ND = 83.00016.K11

D6001

Do Not Stuff

Do Not Stuff

DY

R6002

Do Not Stuff

DY

R6006

510R2J-1-GP

+RTC_PWR

RTC1

ACES-CON2-29-GP

20.F1639.002

2nd = 20.F1804.002

3D3V_AUX_S5

SPICS# is push-pull pin,

SPI_HOLD#

10K R22 1/3-GP

R6002

R6004

Do Not Stuff

27 SPICS#

27 SPIDI

27 SPI_WP2#

150R2F-1-GP1

ER6001

SPI_DI

SPI_WP2#

U6002

CE#

SO

WP#

GND

VCC

HOLD#

SCK

SIO

PM25L020C-SCE-Gr

72.25020.E01

2nd = 72.25020.00D

256KB

3D3V_AUX_S5

ER6004

Do Not Stuff

C6004

SCD22U25V3KX-GP

150R2F-1-GP1

ER6003

ER6002

SPI_CLK

SPI_D0

SPICLK

SPI_D0

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Flash/RTC

Rev

BA40-HR

Sheet 60 of 109

SSID = USB

D12G

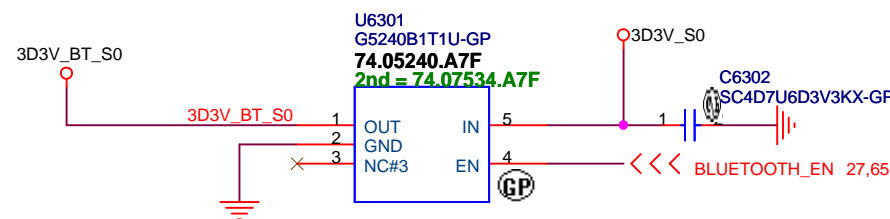
<div>緯創資通</div> <div>Wistron Corporation</div> <div>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</div>		
Title <div>USB Power SW</div>		
Size <div>A4</div>	Document Number <div>BA40-HR</div>	Rev <div>SD</div>
Date <div>Thursday, April 07, 2011</div>		Sheet <div>61</div> of <div>109</div>

D12G

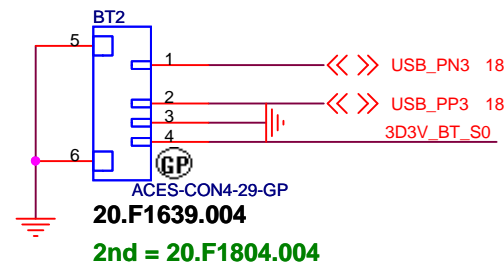
<div>緯創資通</div>		<div>Wistron Corporation</div>	
<div>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</div>			
<div>Title</div>			
<div>USB 3.0 Port</div>			
<div>Size</div>	<div>Document Number</div>		<div>Rev</div>
<div>A3</div>	<div>BA40-HR</div>		<div>SD</div>
<div>Date:</div>	<div>Thursday, April 07, 2011</div>		<div>Sheet 62 of 109</div>

SSID = User.Interface
Bluetooth Module conn.

ANNIE Bluetooth Module

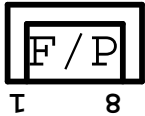


EC6302 put near BLUE1 / all USB put one
choke near connector by EMI request



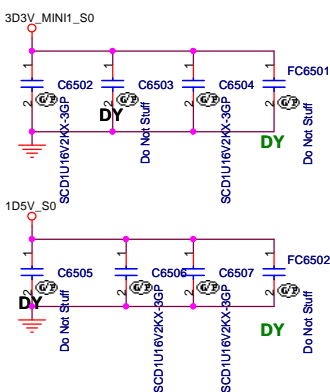
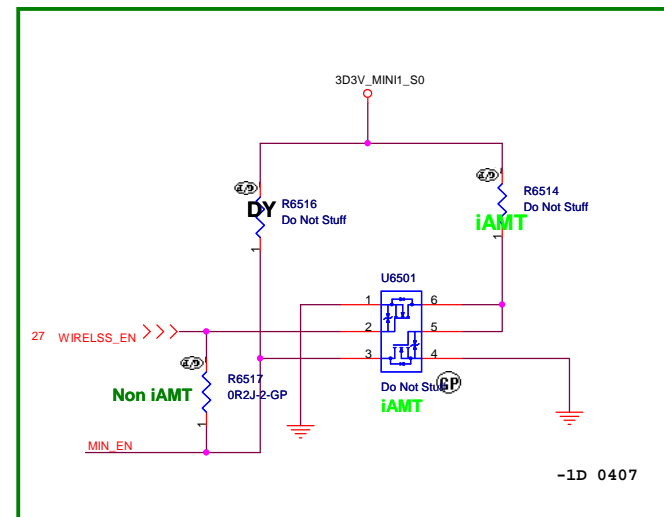
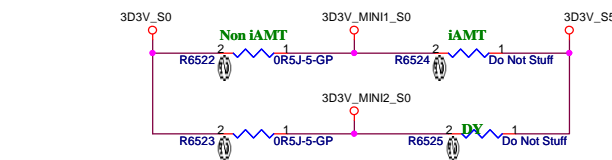
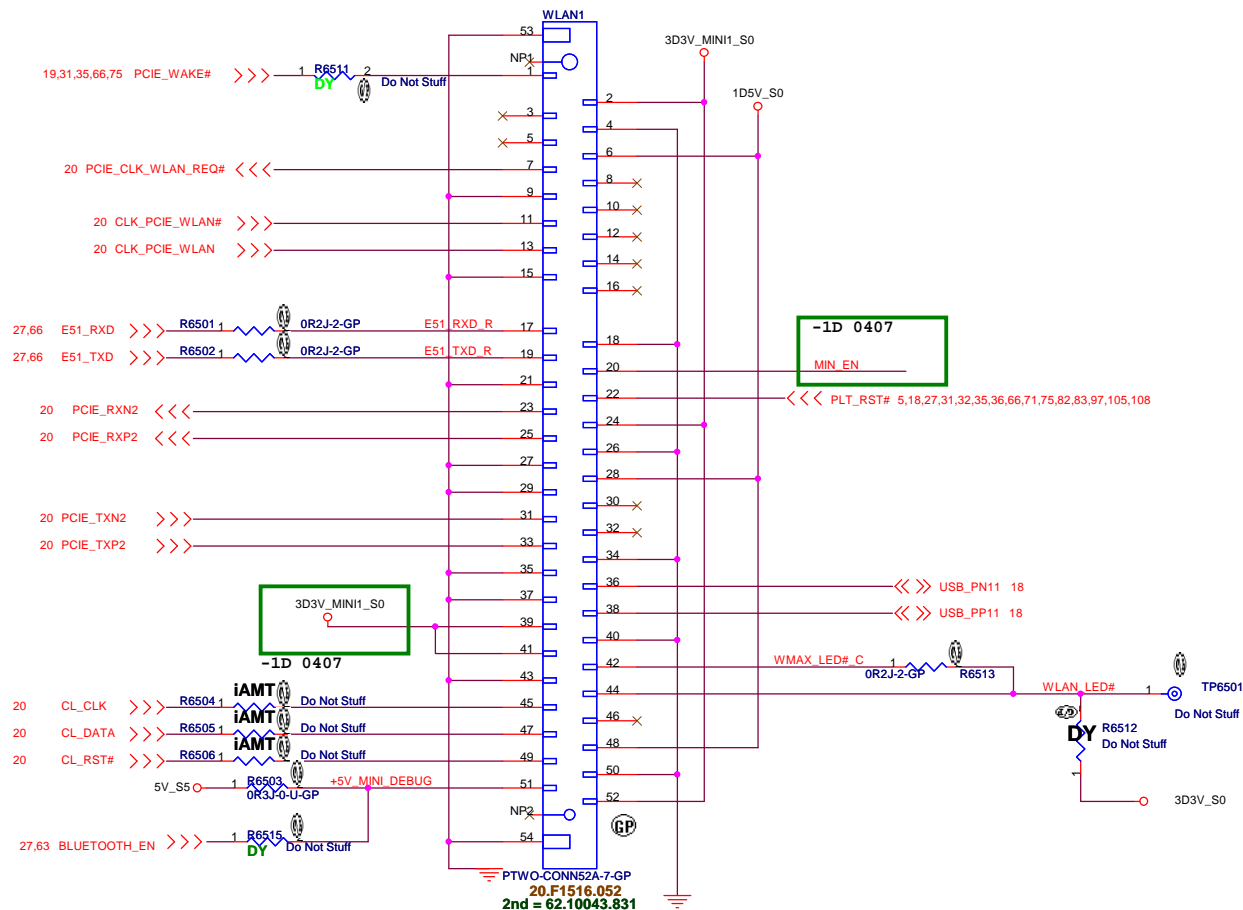
Finger printer

JE40 delete FP function



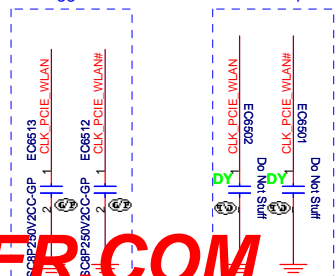
SSID = Wireless

Mini Card Connector(802.11a/b/g/n)



RF suggestion

EMI request



WWW.ALISALER.COM

D12G

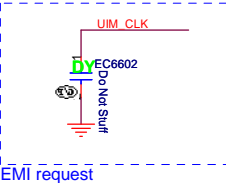
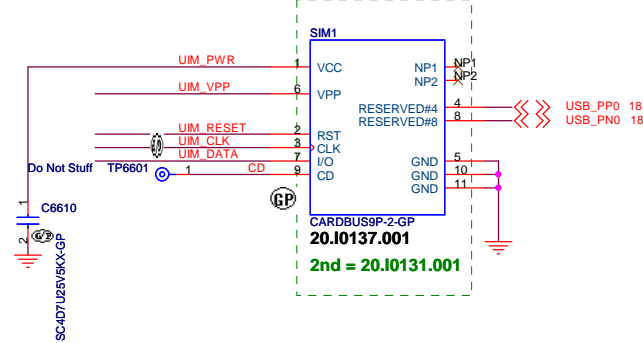
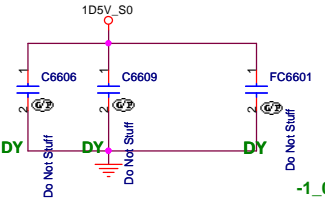
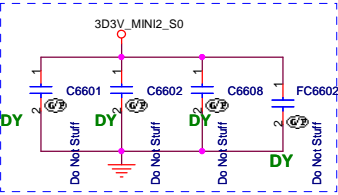
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title			MINICARD(WLAN)/TP CONN
Size	Document Number	Rev	SD
A3	BA40-HR		
Date:	Thursday, April 07, 2011	Sheet	65 of 109

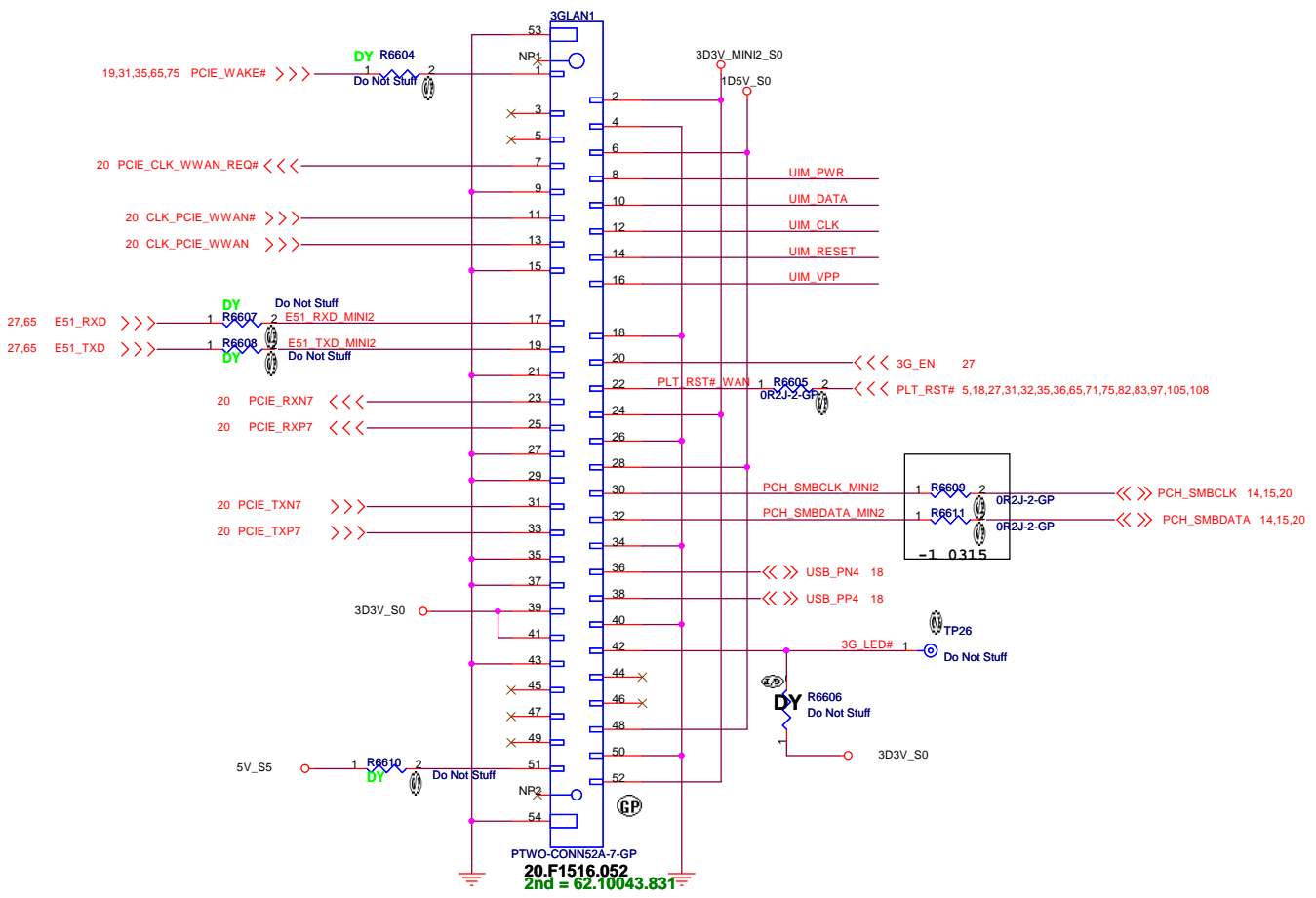
SSID = Wireless

20100712 V1.5

Place near MINI Card CONN



Mini Card Connector(WWAN)



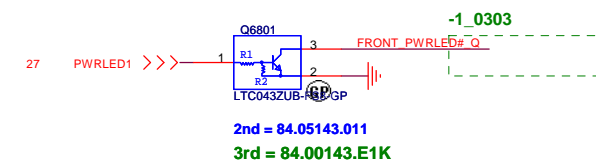
WWW.ALISALER.COM

(Blanking)

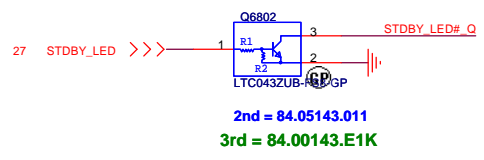
D12G

<div>緯創資通</div>		<div>Wistron Corporation</div>	
		<div>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</div>	
<div>Title</div>			
<div>Reserved</div>			
<div>Size</div>	<div>Document Number</div>		<div>Rev</div>
<div>A4</div>	<div>BA40-HR</div>		<div>SD</div>
<div>Date: Thursday, April 07, 2011</div>		<div>Sheet</div>	<div>67 of 109</div>

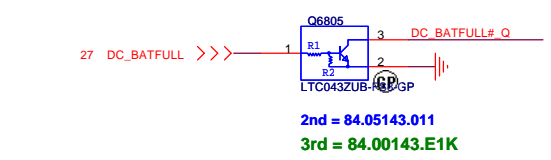
Power button LED



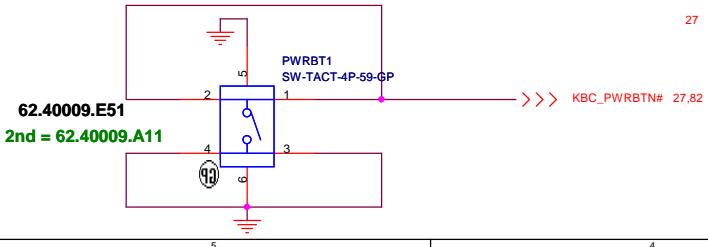
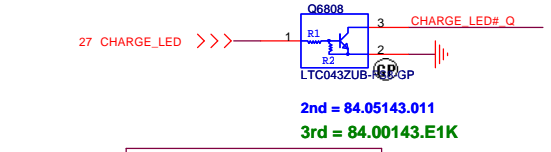
Power STDBY_LED



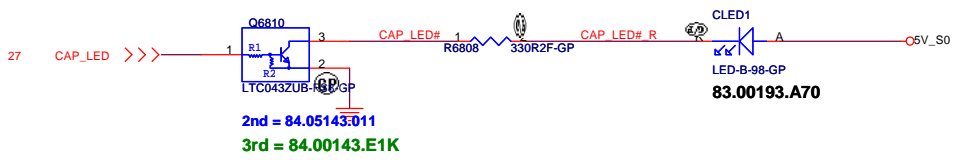
Battery LED2(DC_BATFULL)



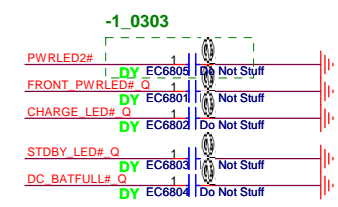
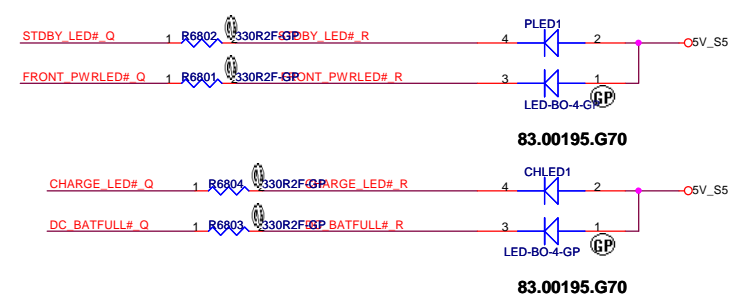
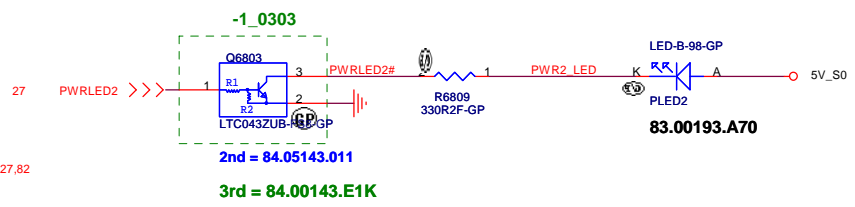
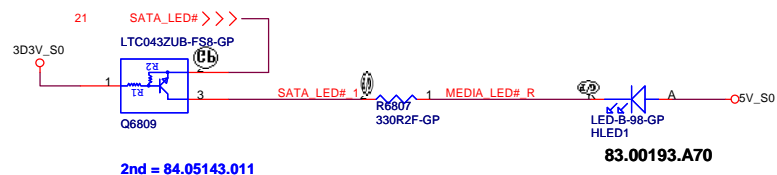
Battery LED1(CHARGE)



Caps Lock LED



SATA HDD LED



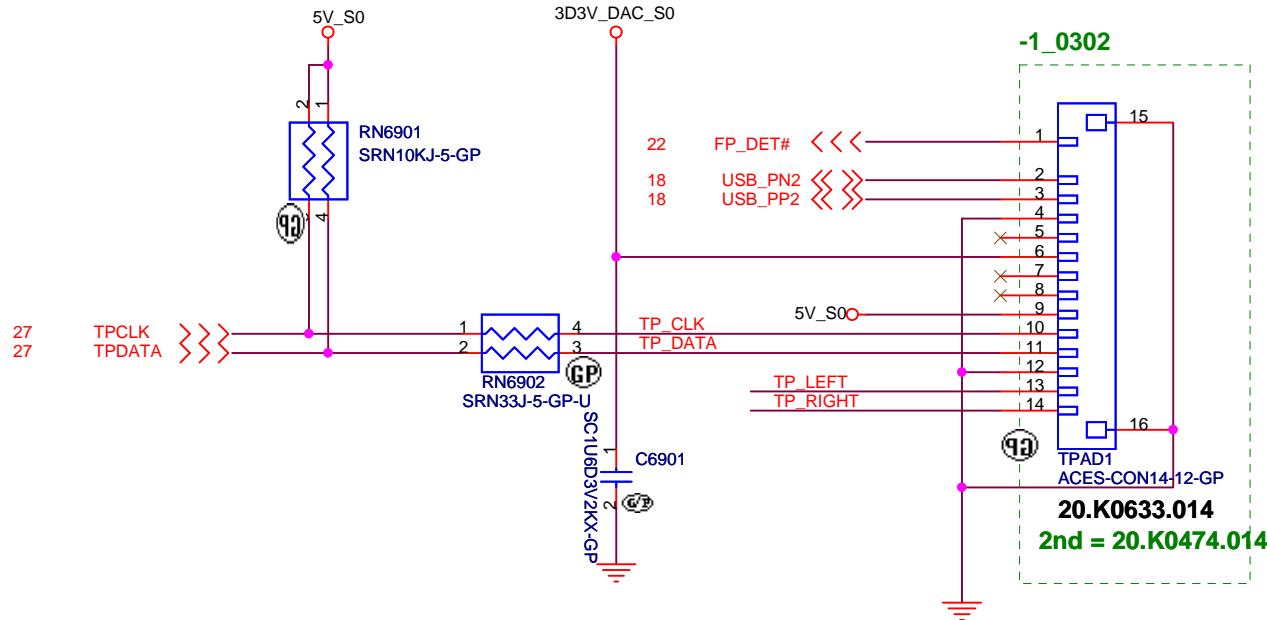
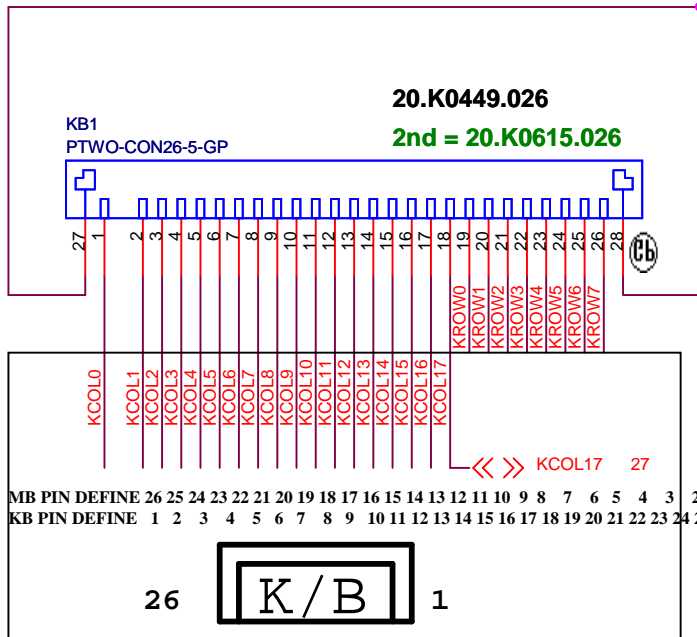
for factory test

D12G		Wistron Corporation	
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		LED Bard/Power Button	
Title		BA40-HR	
Size		SD	
Custom		Rev	
Date: Thursday, April 07, 2011		Sheet 68 of 109	

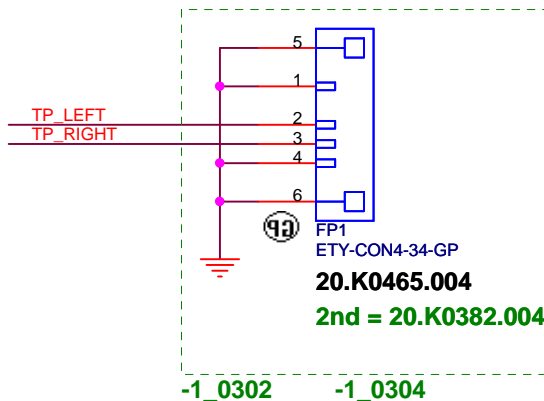
SSID = KBC

TOUCH PAD

Internal KeyBoard Connector



Rubber Dome



WWW.ALISALER.COM

D12G

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title
Key Board/Touch Pad

Size A4 Document Number
BA40-HR

Date: Thursday, April 07, 2011 Sheet 69 of 109

Rev
SD

5

4

3

2

1

D

D

C

C

B

B

A

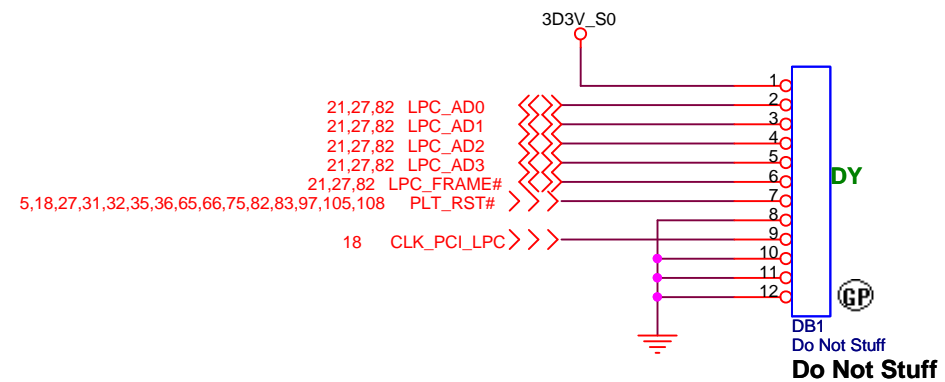
A

WWW.ALISALER.COM

D12G

<div><div>緯創資通</div><div>Wistron Corporation</div><div>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</div></div>		
Title <div>Hall Sensor</div>		
Size <div>A4</div>	Document Number <div>BA40-HR</div>	Rev <div>SD</div>
Date: Thursday, April 07, 2011		Sheet 70 of 109

SB modify to test pad



D12G

緯創資通

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

Dubug connector

Size
A4

Document Number

BA40-HR

Rev
SD

Date: Thursday, April 07, 2011

Sheet 71 of 109

WWW.ALISALER.COM

(Blanking)

D12G

緯創資通

Wistron Corporation

21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

Size
A3

Document Number
BA40-HR

Date: Thursday, April 07, 2011

Rev
SD

Sheet 72 of 109

(Blanking)

D12G

緯創資通

Wistron Corporation

21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

Reserved

Size
A3

Document Number
BA40-HR

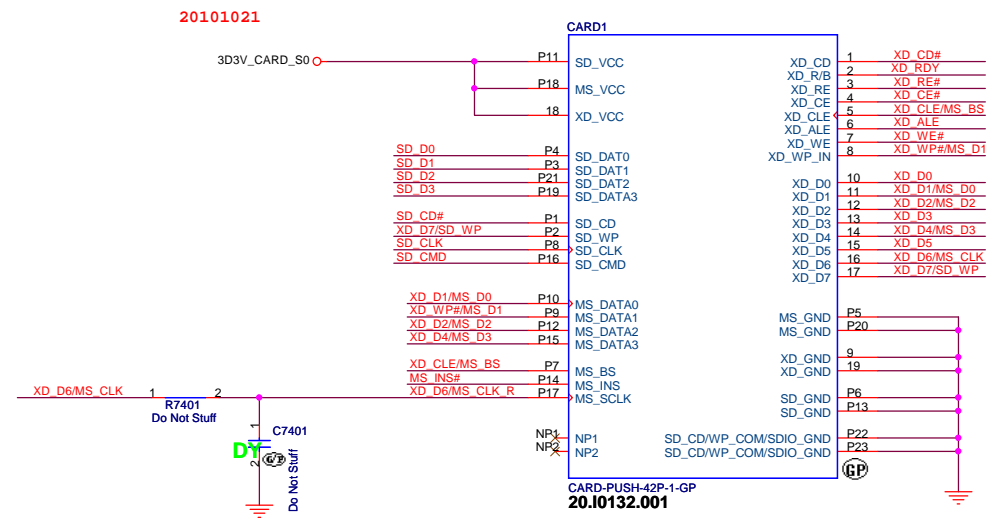
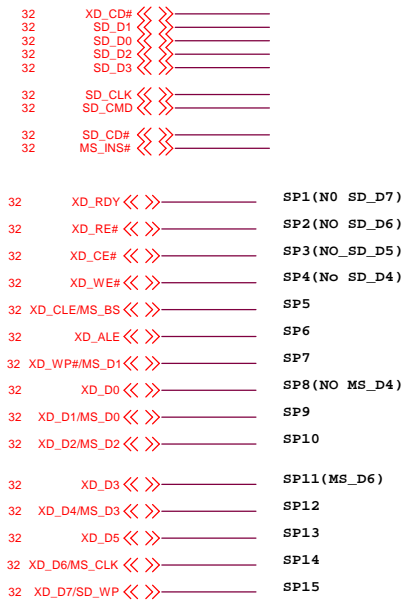
Date: Thursday, April 07, 2011

Rev
SD

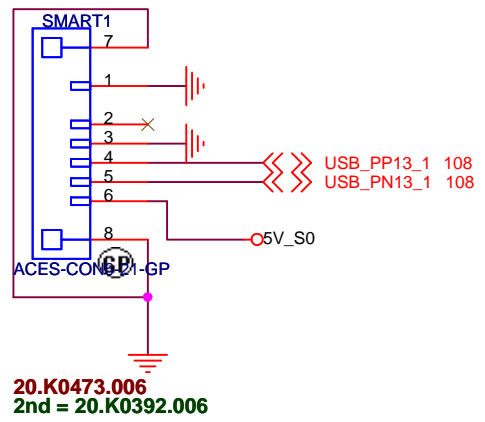
Sheet 73 of 109

SD/XD/MS Card Reader

SSID = SDIO



WWW.ALISALER.COM



D12G

緯創資通		Wistron Corporation	
		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
Reserved			
Size A4	Document Number BA40-HR		Rev SD
Date:	Thursday, April 07, 2011	Sheet 76 of	109

D12G

<div>緯創資通</div>		<div>Wistron Corporation</div>	
<div>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</div>			
<div>Title</div>			
<div>Reserved</div>			
<div>Size</div>	<div>Document Number</div>		<div>Rev</div>
<div>A3</div>	<div>BA40-HR</div>		<div>SD</div>
<div>Date:</div>	<div>Thursday, April 07, 2011</div>		<div>Sheet 77 of 109</div>

(Blanking)

D12G

緯創資通		Wistron Corporation	
		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
Reserved			
Size	Document Number		Rev
A4	BA40-HR		SD
Date: Thursday, April 07, 2011		Sheet 78 of	109

SSID = User.Interface

Free Fall Sensor

Note

- no via, trace, under the sensor (keep out area around 2mm)
- stay away from the screw hole or metal shield soldering joints
- design PCB pad based on our sensor LGA pad size (add 0.1mm)
- solder stencil opening to 90% of the PCB pad size
- mount the sensor near the center of mass of the NB as possible as you can

JE40 delete G Sensor Function

Note

- (1) Keep all signals are the same trace width. (included VDD, GND).
- (2) No VIA under IC bottom.

WWW.ALISALER.COM

D12G

緯創資通

Wistron Corporation

21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

Free Fall Sensor

Size
A4

Document Number

BA40-HR

Rev
SD

Date: Thursday, April 07, 2011

Sheet 79 of 109

(Blanking)

D12G

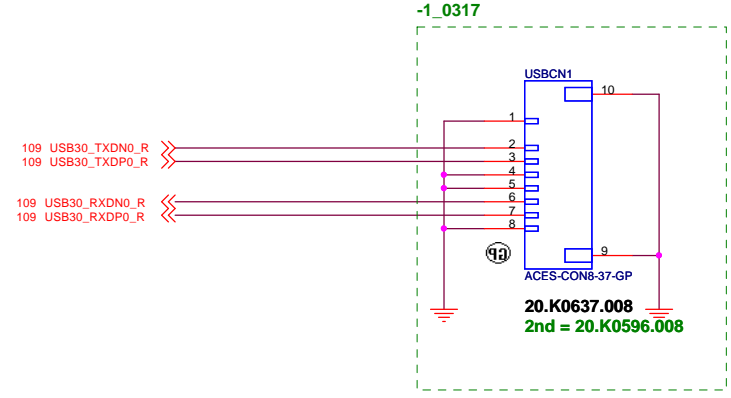
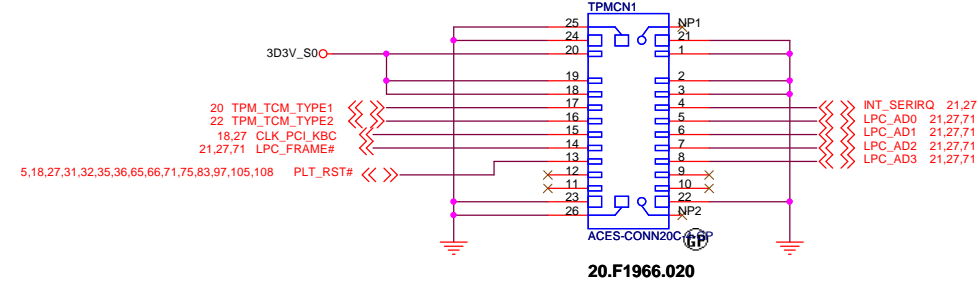
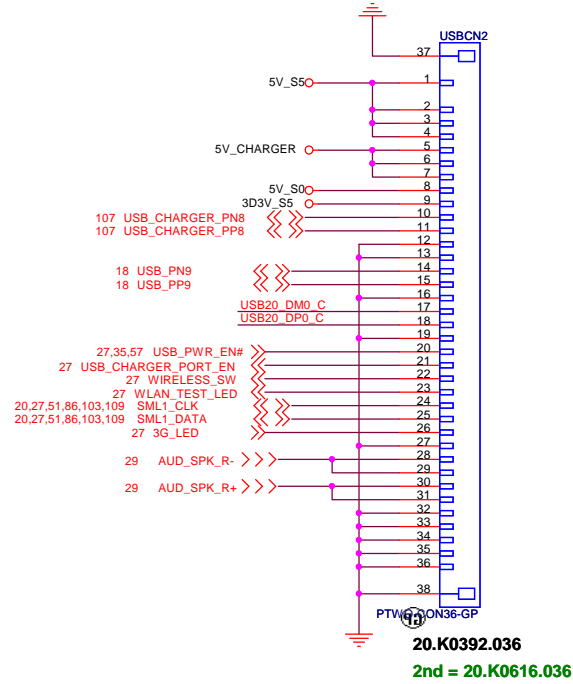
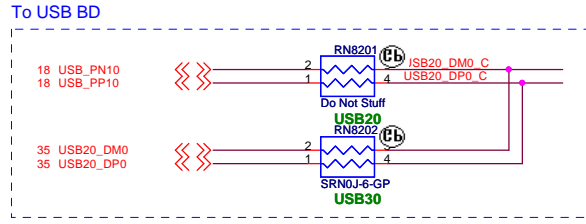
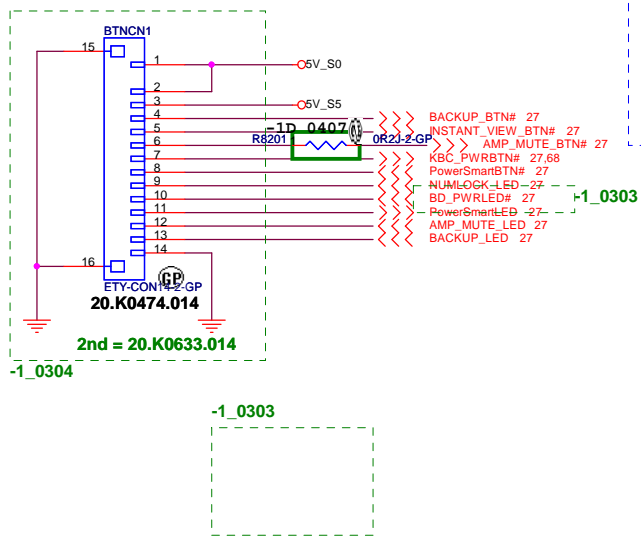
<div>緯創資通Wistron Corporation</div> <div>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</div>		
TitleReserved		
SizeA4	Document NumberBA40-HR	RevSD
Date: Thursday, April 07, 2011		Sheet 80 of 109

(Blanking)

D12G

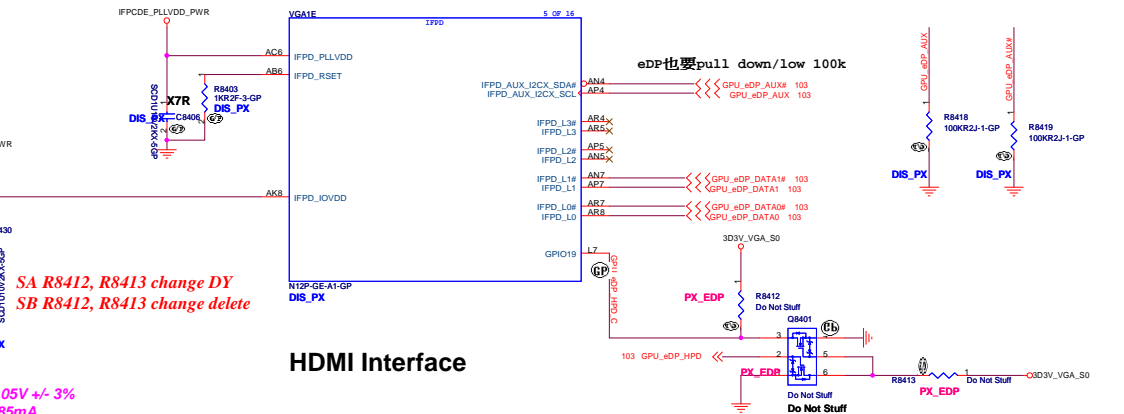
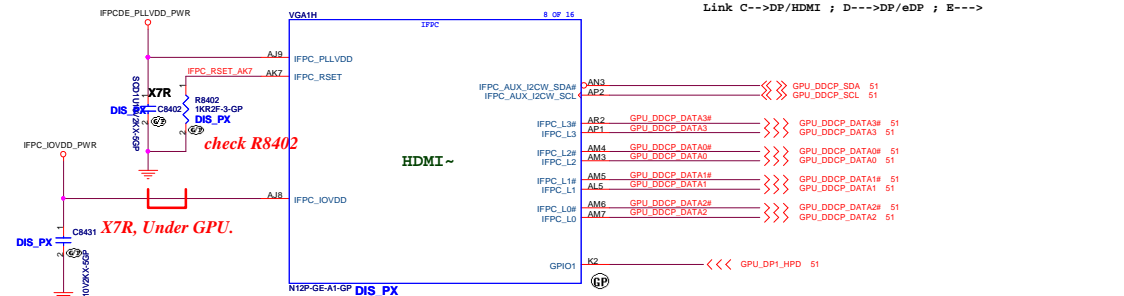
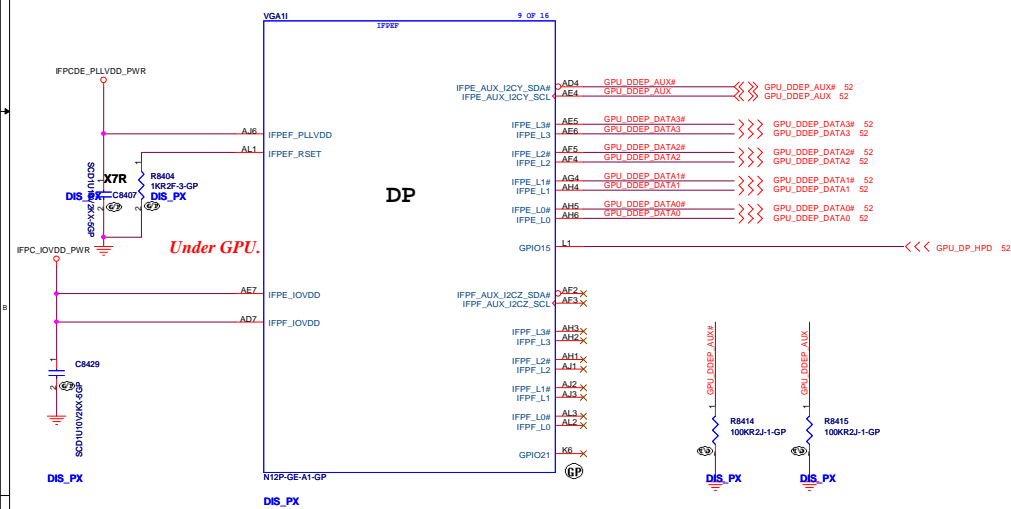
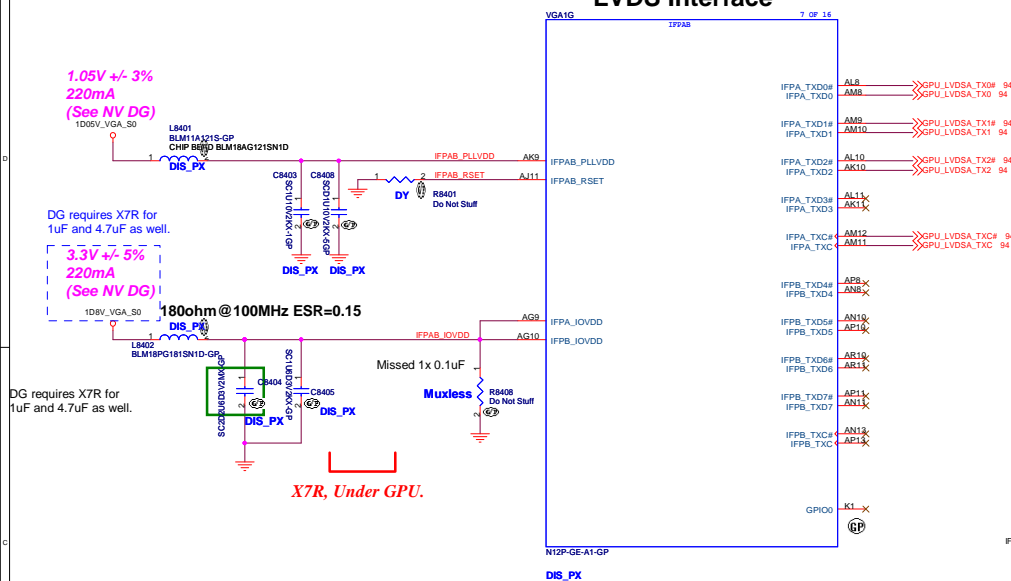
<div>緯創資通</div>		<div>Wistron Corporation</div>	
		<div>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</div>	
<div>Title</div>			
<div>Reserved</div>			
<div>Size</div>	<div>Document Number</div>		<div>Rev</div>
<div>A4</div>	<div>BA40-HR</div>		<div>SD</div>
<div>Date: Thursday, April 07, 2011</div>		<div>Sheet 81 of</div>	<div>109</div>

PWRCN1 FFC 異面

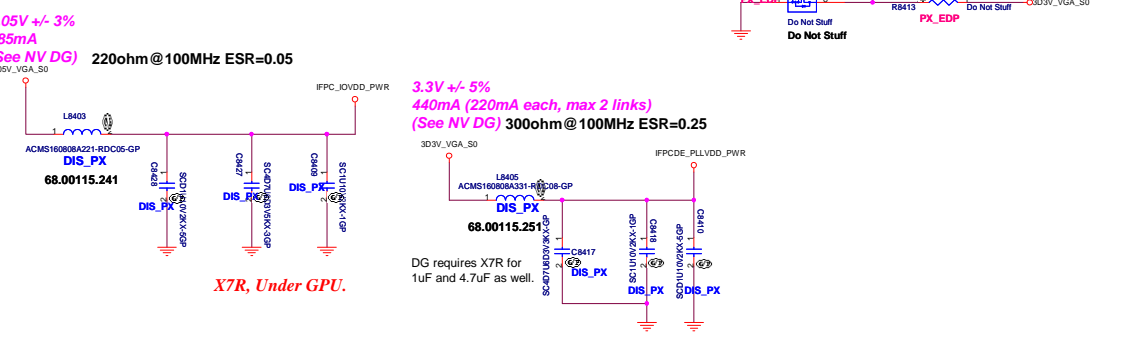


WWW.ALISALER.COM

LVDS Interface



HDMI Interface



EDP 10A

DC tolerance +/- 75mV
AC tolerance +/- 50mV < 100MHz

X7R, Under GPU.

X7R, Near GPU.

1.05V +/- 3%
200mA
(See NV DG)

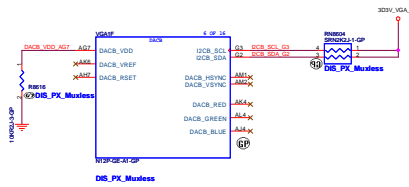
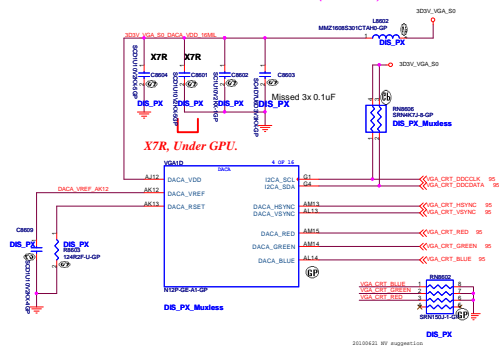
X7R, Under GPU.

FBCLK Termination place on VRAM side

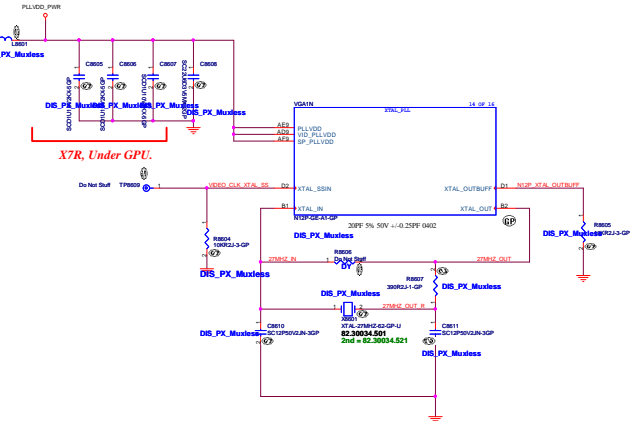
FBCLK Termination place on VRAM side

300ohm @ 100MHz ESR=0.25ohm

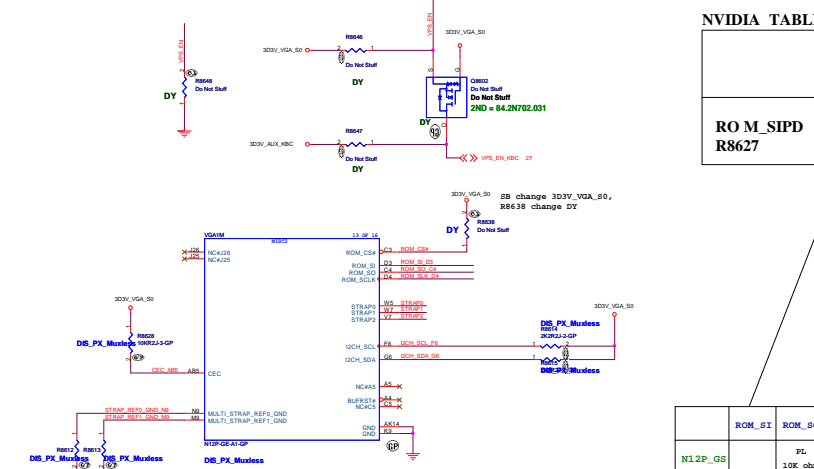
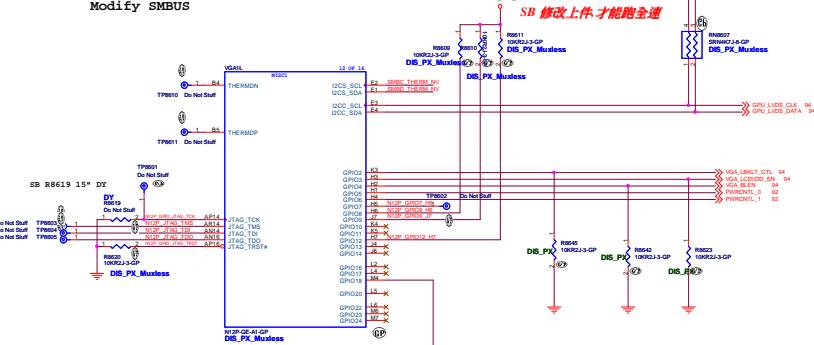
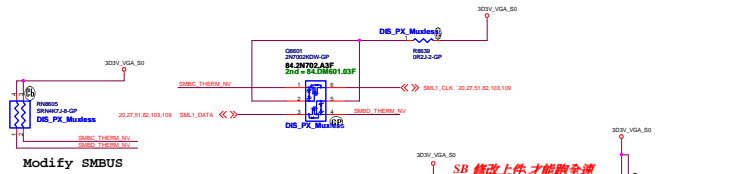
3.3V +/- 3%
120mA
(See NV DG)



1.05V +/- 3%
150mA
(See NV DG)



VGA Thermal sensor P2800



N12P-GS			
P-State	PWR_VGA_CORR_D1	PWR_VGA_CORR_D0	VGA_CORR_PWR
L	L	L	0.25V
H	H	L	0.9V
L	H	H	0.975V
H	H	H	1V

default boot voltage table

Configuration	Vendor	Straps	Manufacturer Part Number	Speed Bin (MHz)
S4x16 DDR3	Hynix	0x2	H5TQ1G63DFR-11C	800/800
	Samsung	0x3	K4W1G1646E-BC11	800
	Samsung	7BD	K4W1G1646G-BC11	800/800
	Hynix	0x0	H5TQ1G63DFR-12C	800
	Samsung	0x1	K4W1G1646E-BC12	800

NVIDIA TABLE

	Hynix 2G 0010 128*16*8	Hynix 1G 0010 64*16*8 800MHZ	Samsung 1G 0011 64*16*8 800MHZ	Samsung 512 64*16*8 800MHZ	Samsung 2G 0111 128*16*8 800MHZ
RO M_SIPD R8627	34.8Kohm 64.34825.6DL	15Kohm 64.15025.6DL	20Kohm 64.20025.6DL	20Kohm 64.20025.6DL	45Kohm 64.45325.6DL

	ROM_S1	ROM_S0	ROM_CLK	STRAP0	STRAP1	STRAP2
N12P_GS	PL	PL	PL	PL	PL	PL
N12P_GV	PL	PL	PL	PL	PL	PL

TABLE NVIDIA

	71.0N12P.E0U	71.0N12P.A0U			
	N12P-GS DEV ID: 0x0DF4	N12P-GV DEV ID: 0x0DF7	N11P-GE Fermi DEV ID: 0x0DF1 (0001)	N11P-GS Fermi DEV ID: 0x0DF0 (0000)	N12P-GE DEV ID: 0x0DF5 (0101)
STRAP2	25Kohm 64.24925.6DL	45Kohm 64.45325.6DL	10Kohm 63.10334.1DL	5Kohm 64.49915.6DL	30Kohm 64.30025.6DL

N12P-GS
USE 1111 (45K)

N12P-GV

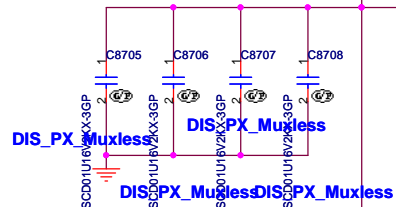
N11P-GE
Pull Low

N11P-GS
Pull Low

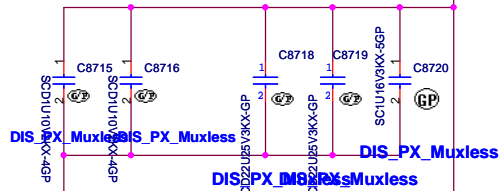
N12P-GE

WWW.ALISALER.COM

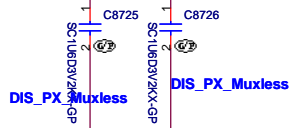
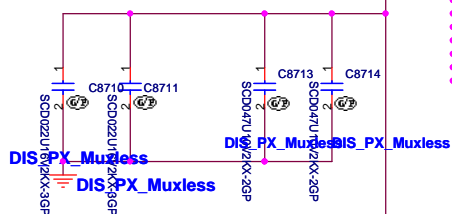
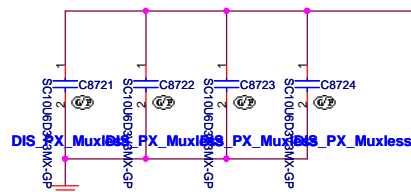
Under GPU



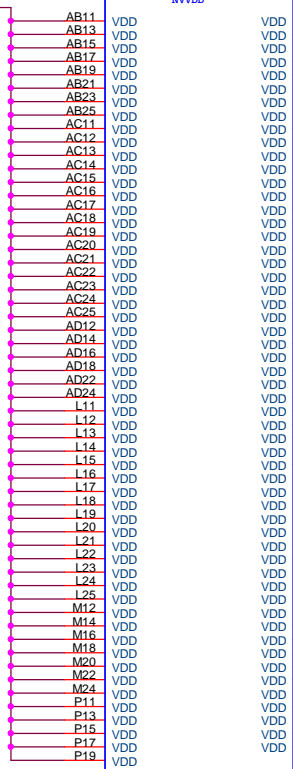
Under GPU



NEAR GPU

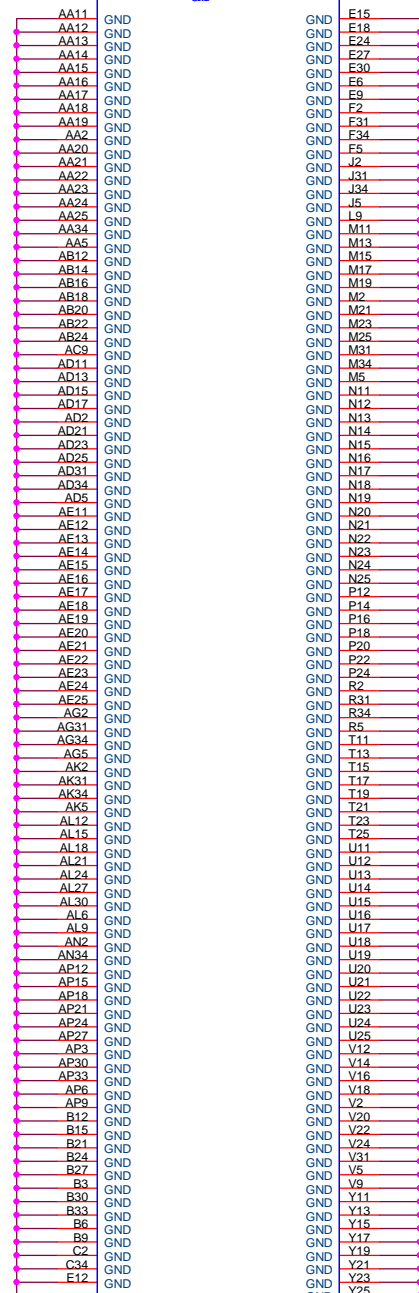


VGA1P 16 OF 16



DIS_PX_Muxless

VGA1O 15 OF 16



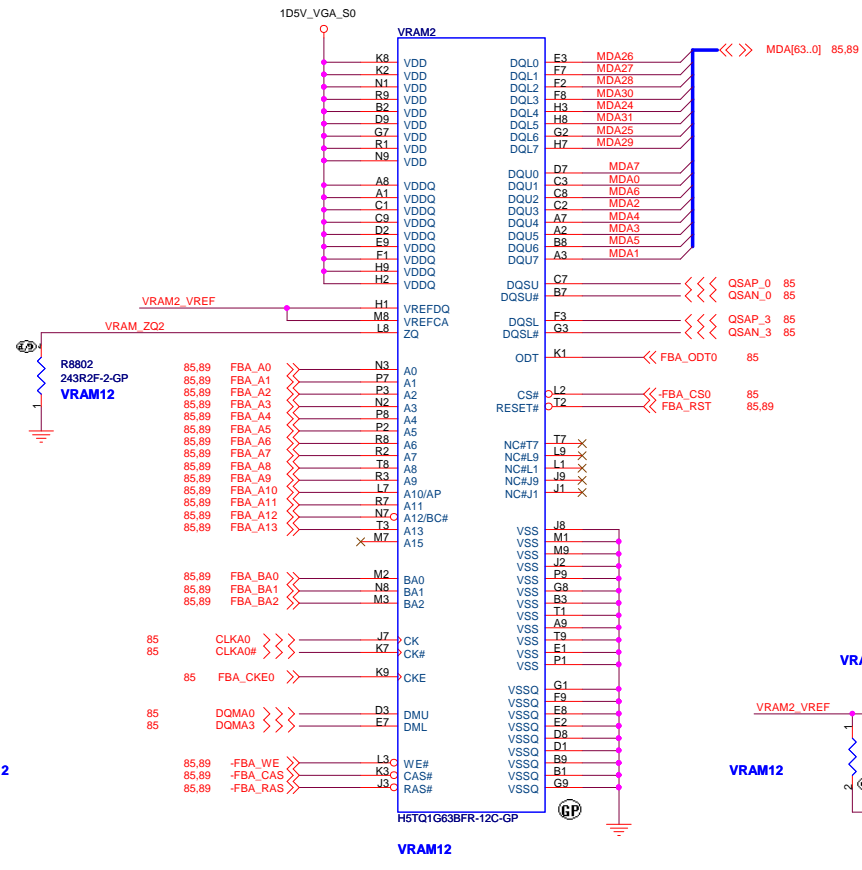
DIS_PX_Muxless

WWW.ALISALER.COM

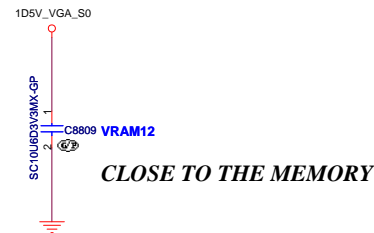
D12G

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

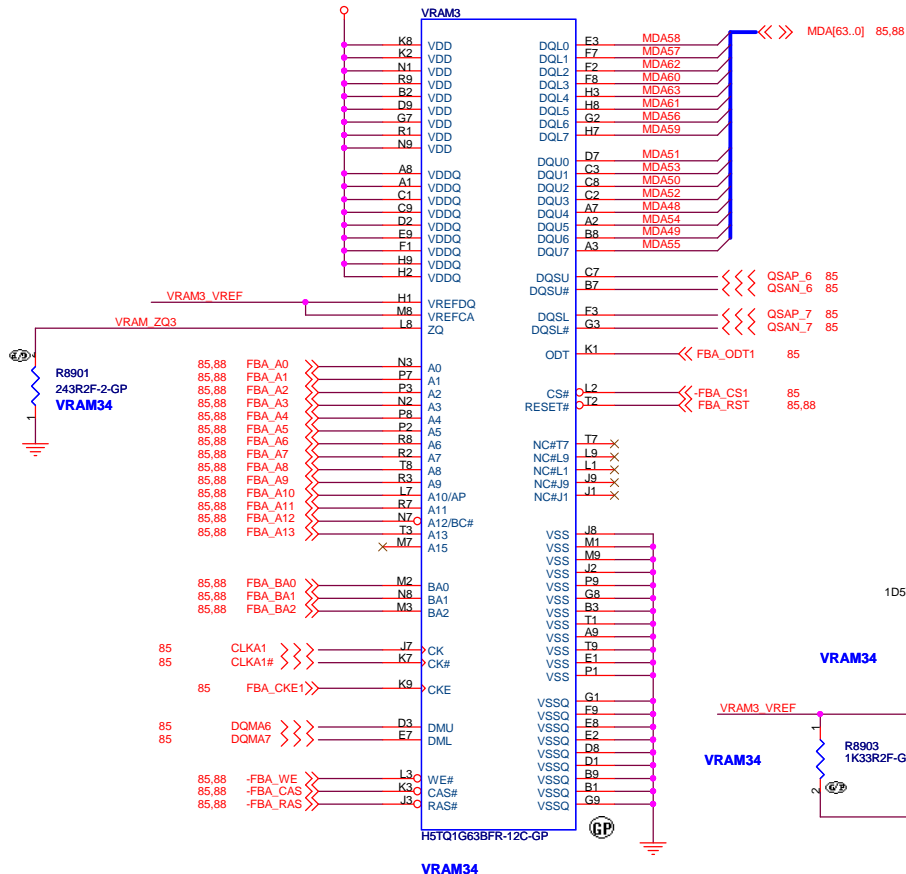
Title GPU DPPWR/GND(5/5)		
Size A3	Document Number BA40-HR	Rev SD
Date: Thursday, April 07, 2011	Sheet 87	of 109



VRAM = Hy2GX8,Sam1GX8,,Hy1GX8,Sam512X4,Sam2Gx8
FB CMD mapping Mode D-N12x



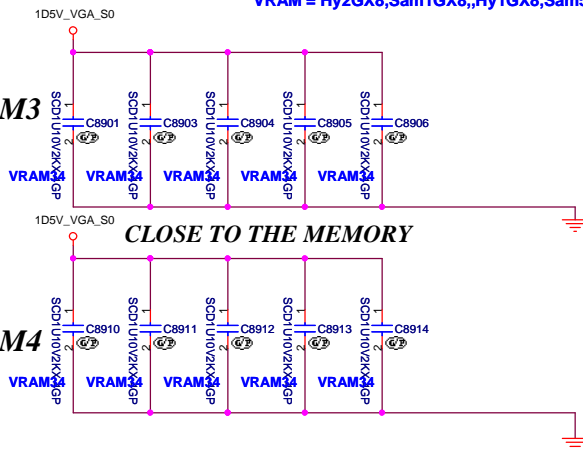
1D5V_VGA_S0



VRAM34

VRAM = Hy2GX8,Sam1GX8,,Hy1GX8,Sam512X4,Sam2Gx8

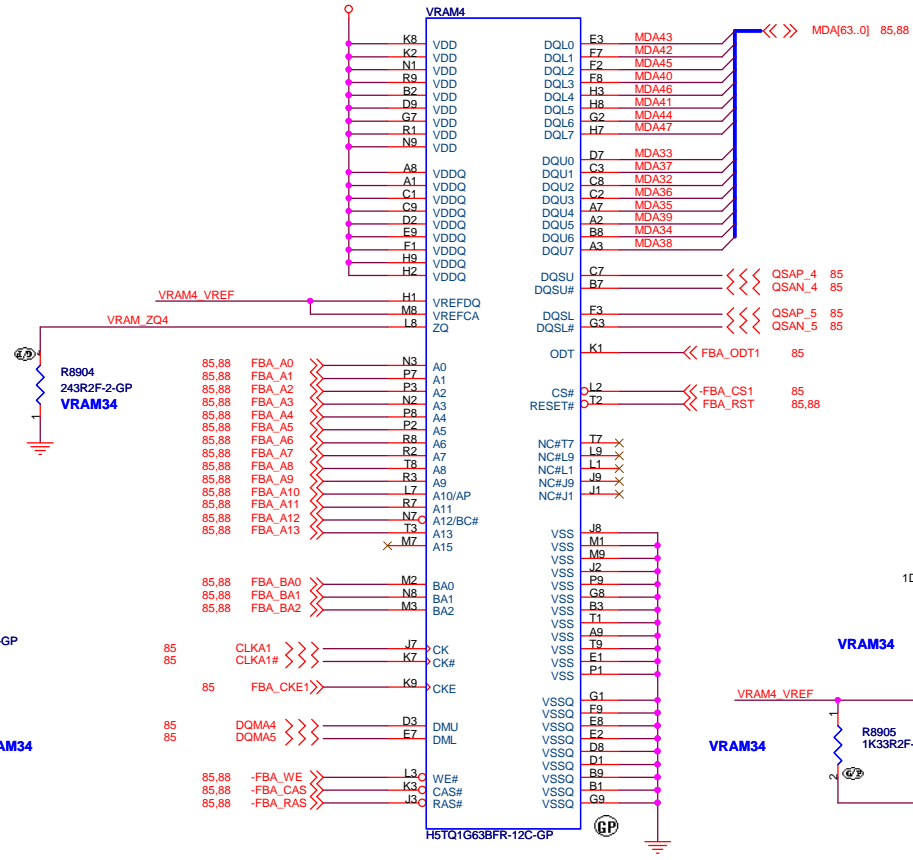
FOR VRAM3



CLOSE TO THE MEMORY

FOR VRAM4

1D5V_VGA_S0



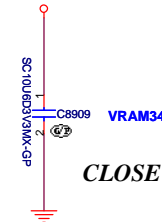
VRAM34

VRAM = Hy2GX8,Sam1GX8,,Hy1GX8,Sam512X4,Sam2Gx8

FB CMD mapping Mode D-N12x

VRAM SAMSUNG 1Gb VR.1GB0B.006
 VRAM HYNIX 1Gb 72.51G63.C0U/VR.1GB0G.005
 VRAM HYNIX 2Gb VR.2GB0G.001

1D5V_VGA_S0

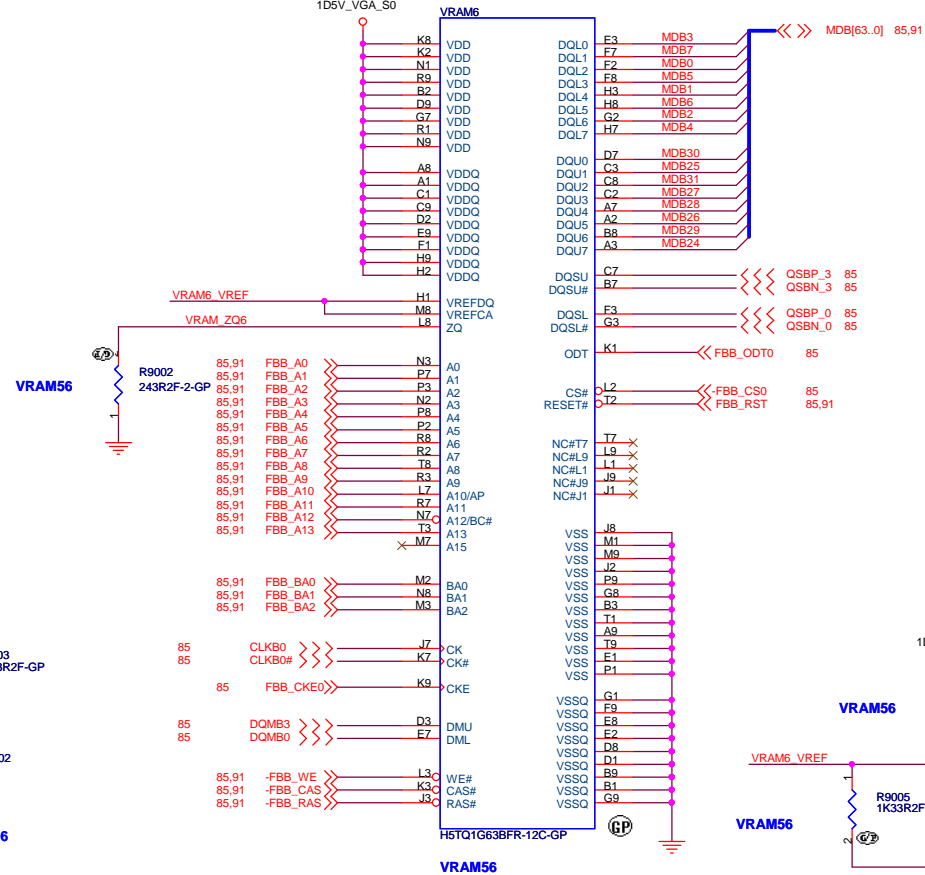


CLOSE TO THE MEMORY

D12G

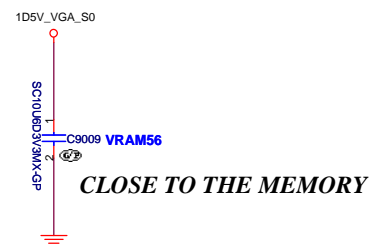
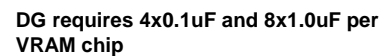
緯創資通 Wistron Corporation
 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
 Taipei Hsien 221, Taiwan, R.O.C.


Title GPU-VRAM3,4 (2/4)
 Size Custom Document Number BA40-HR Rev SD
 Date: Thursday, April 07, 2011 Sheet 89 of 109



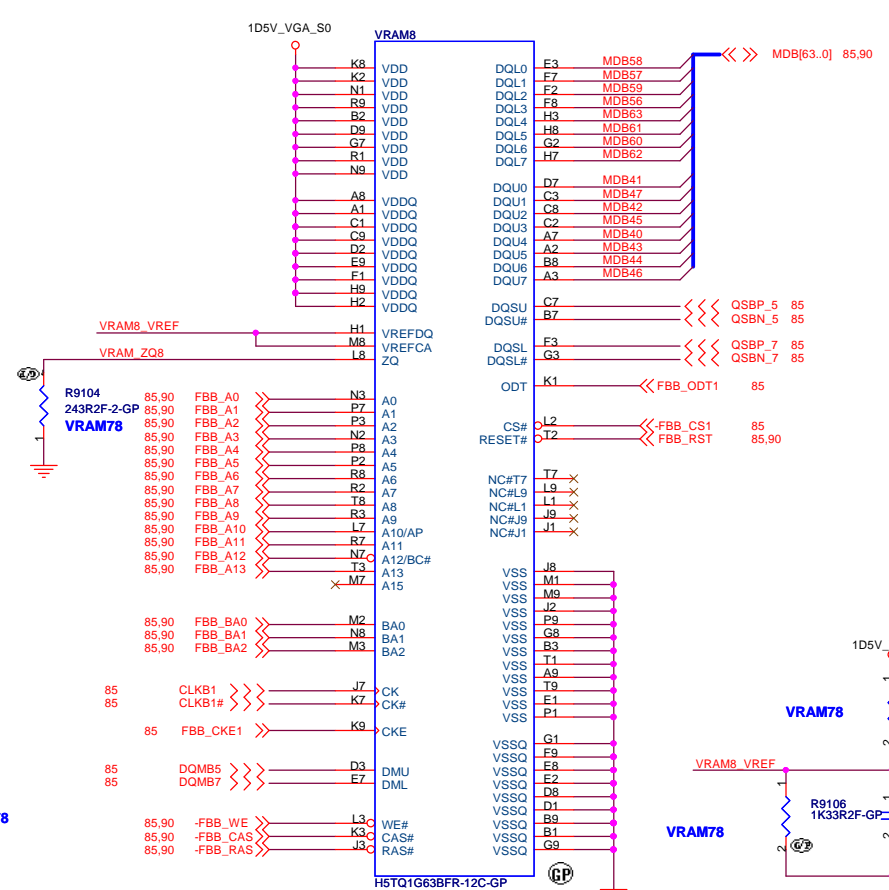
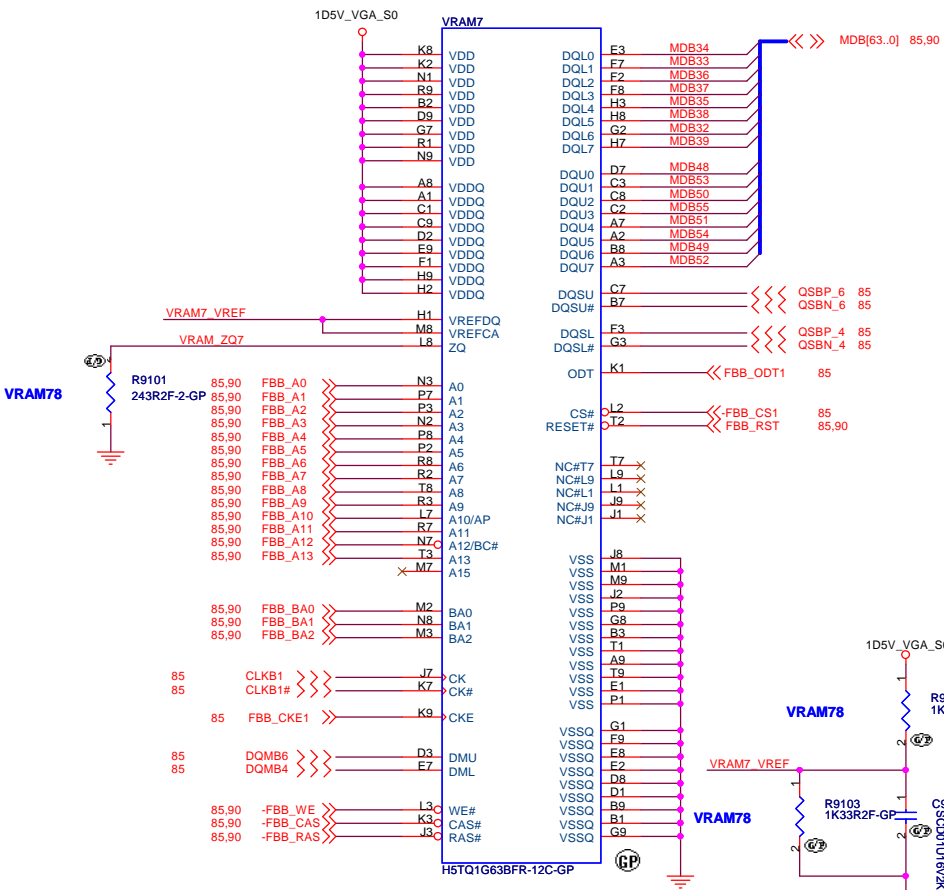
```
VRAM SAMSUNG 1Gb VR.1GB0B.006
VRAM HYNIX 1Gb 72.51G63.C0U/VR.1GB0G.005
VRAM HYNIX 2Gb VR.2GB0G.001
```

VRAM = Hy2GX8,Sam1GX8,Hynix1GX8,Sam2GX8

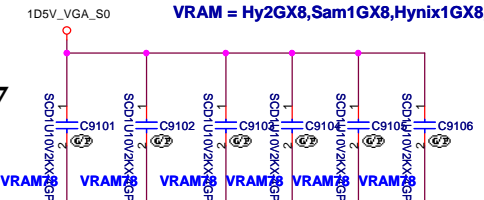


 Wistron Corporation 21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	
GPU-VRAM5.6 (3/4)	
Size	Document Number
Custom	BA40-HR
Date:	Thursday, April 07, 2011
	Sheet 90 of 109
	SD

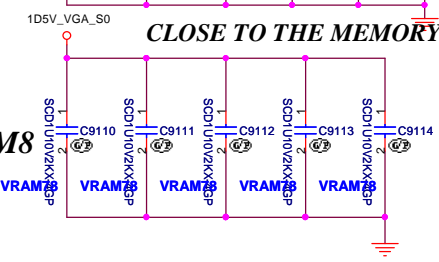
WWW.ALISALER.COM



FOR VRAM7

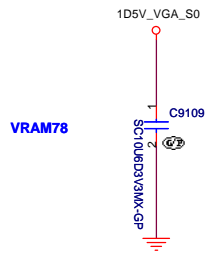


CLOSE TO THE MEMORY



FOR VRAM8

CLOSE TO THE MEMORY

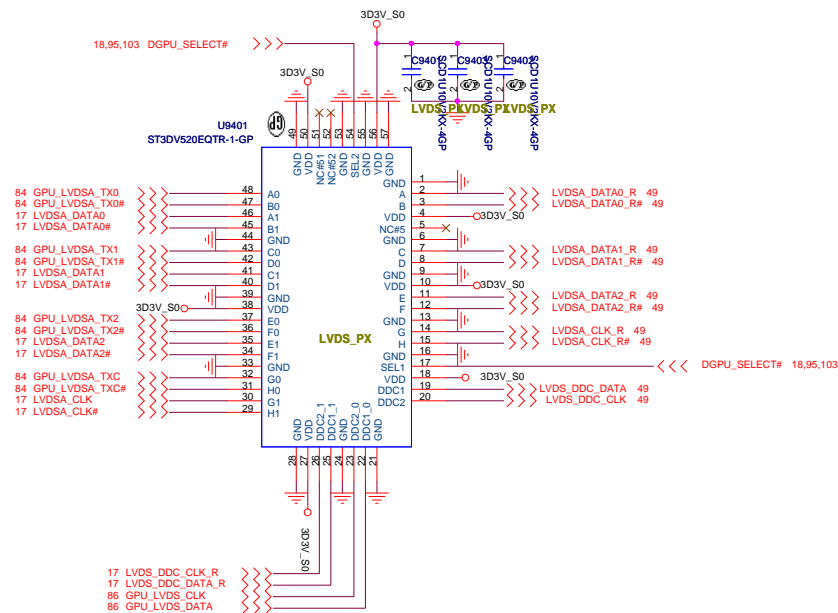


VRAM = Hy2GX8,Sam1GX8,Hynix1GX8,Sam2GX8

VRAM SAMSUNG 1Gb VR.1GB0B.006
VRAM HYNIX 1Gb 72.51G63.C0U/VR.1GB0G.005
VRAM HYNIX 2Gb VR.2GB0G.001



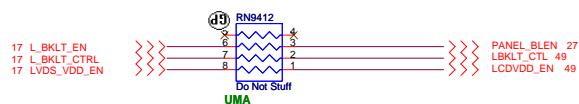
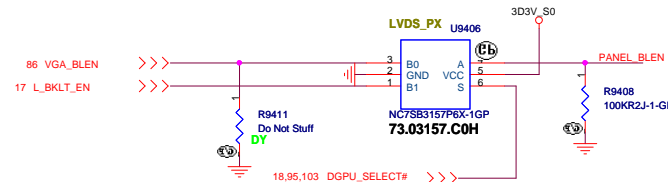
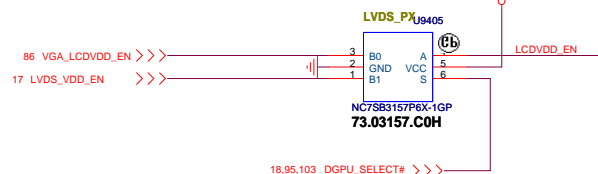
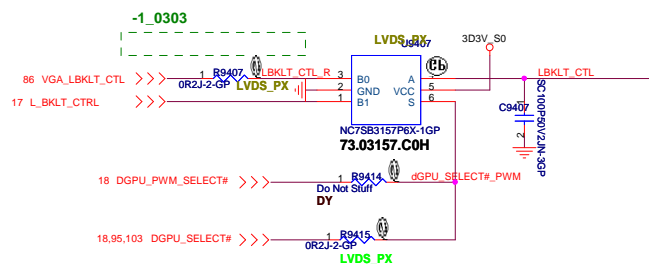
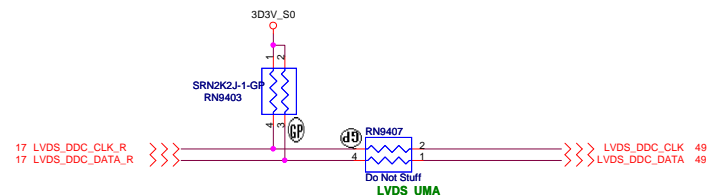
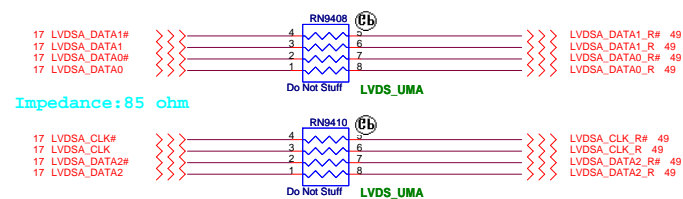
LVDS



SEL->L(X=nX0) , H(X=nX1)

SEL1 Control A~H

SEL2 Control DDC1,DDC2

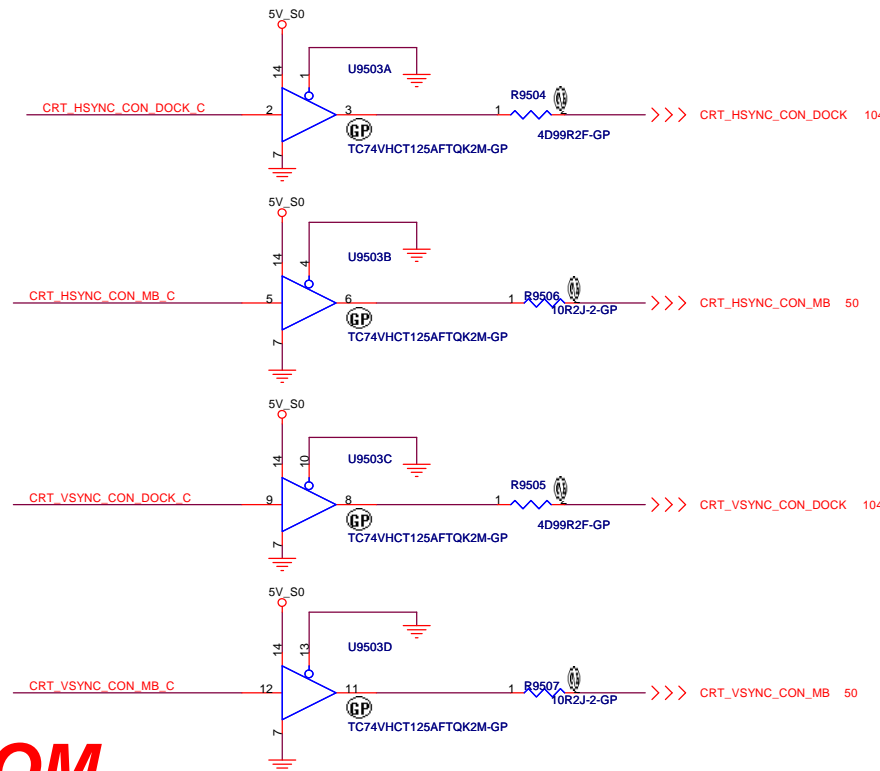
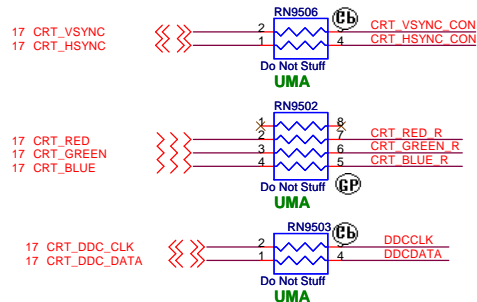
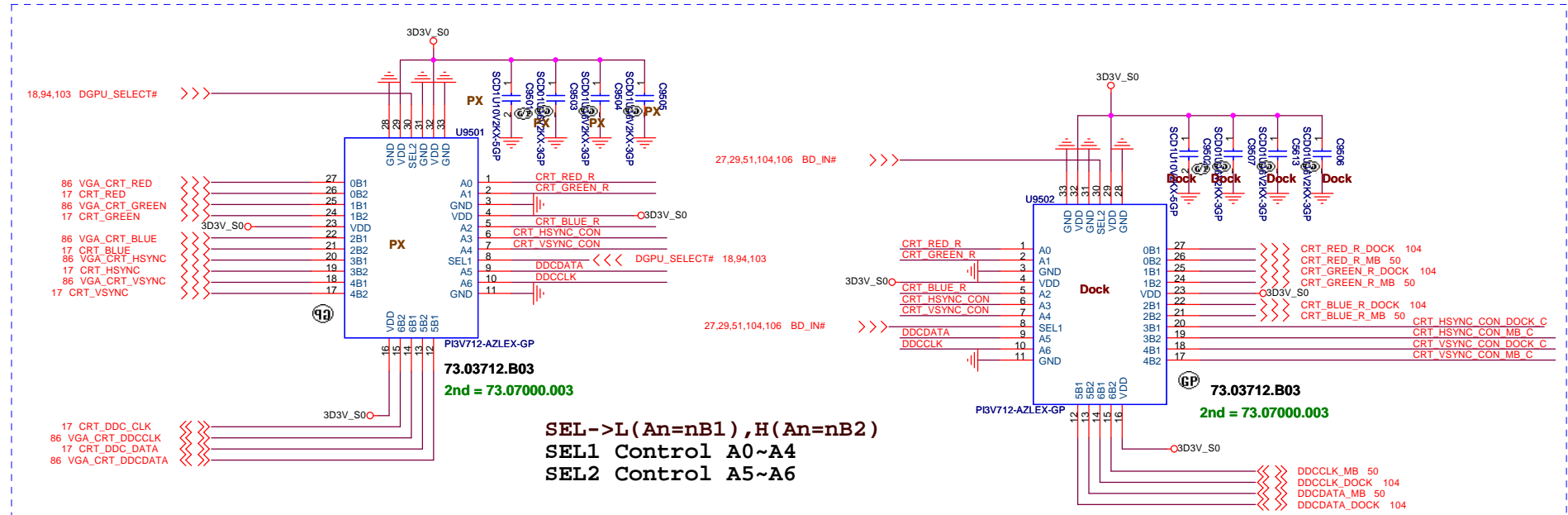


WWW.ALISALER.COM

CRT DDCDATA & DDCCLK

VDD :

Recommend to use 6 caps (0.1u + 5*10nF) close to our chips



WWW.ALISALER.COM

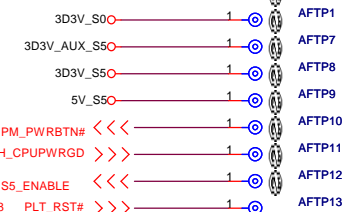
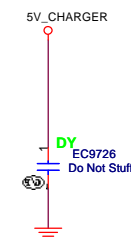
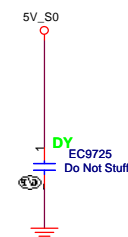
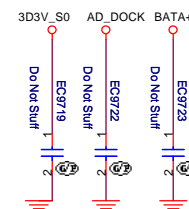
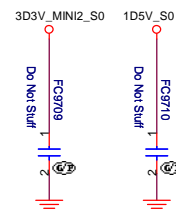
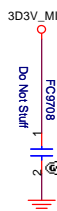
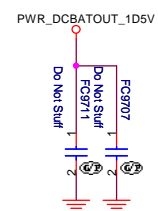
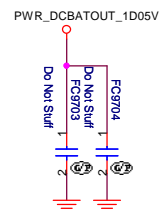
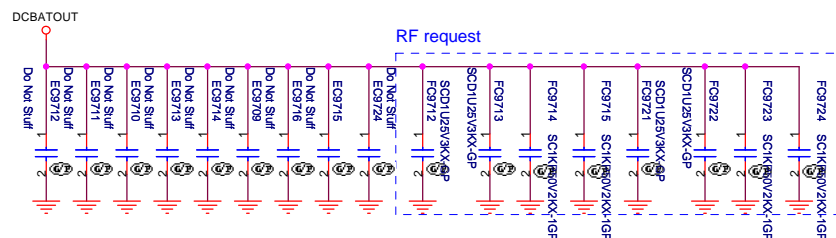
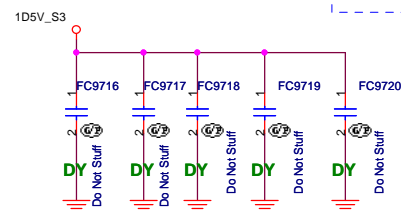
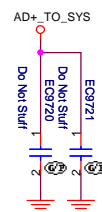
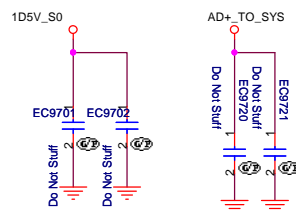
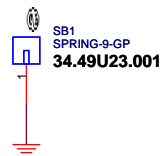
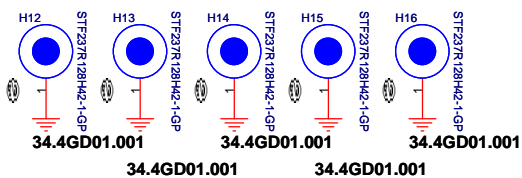
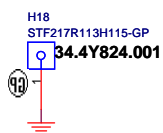
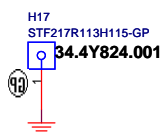
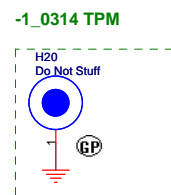
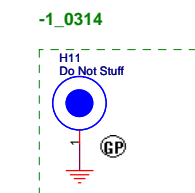
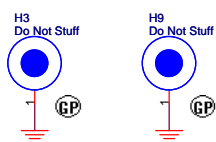
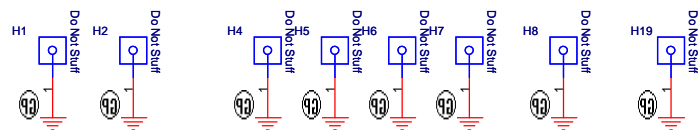
D12G

緯創資通		Wistron Corporation	
		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
CRT Switch			
Size A3	Document Number		Rev
	Huron River		SD
Date:	Thursday, April 07, 2011	Sheet 95 of	109

SSID = SDIO

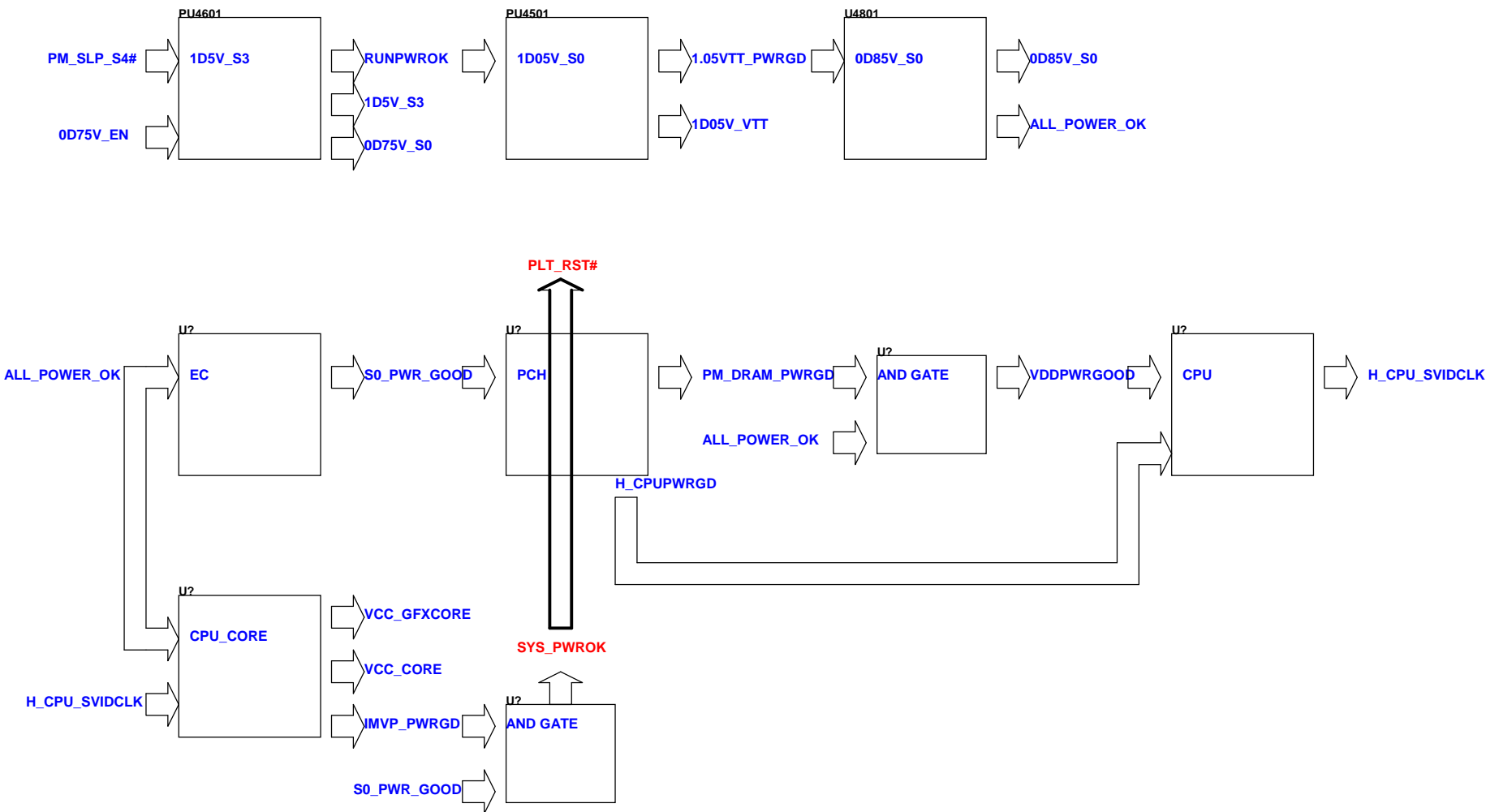
WWW.ALISALER.COM

D12G	
<div>緯創資通Wistron Corporation21F, 88, Sec.1, Hsin Tai Wu Rd., Hsuehshien, Taipei Hsien 221, Taiwan, R.O.C.</div>	
TitleTOUCH PANEL	
SizeA2	Document NumberBA40-HR
DateThursday, April 07, 2011	RevSD
Sheet 96 of 108	



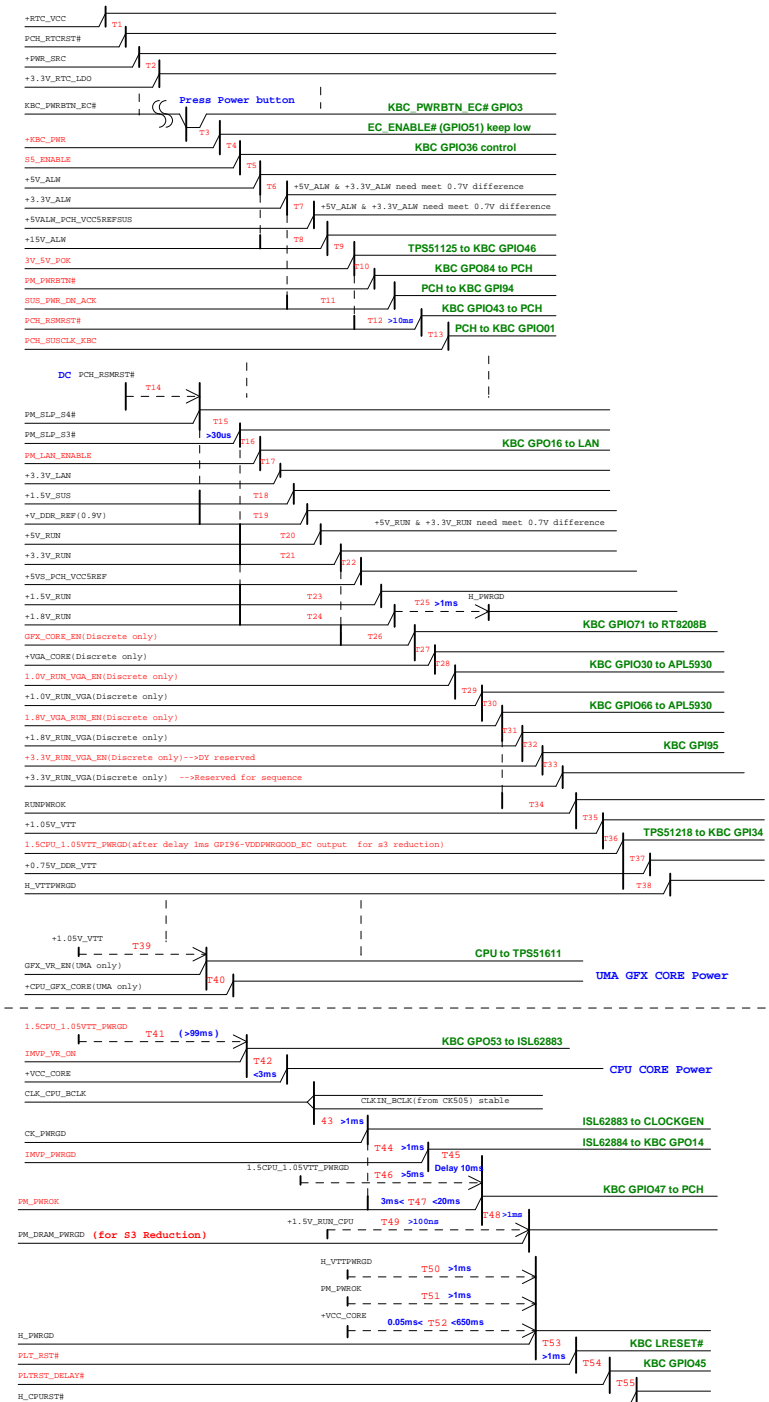
Test Point放在Dimm Door打開可量測處

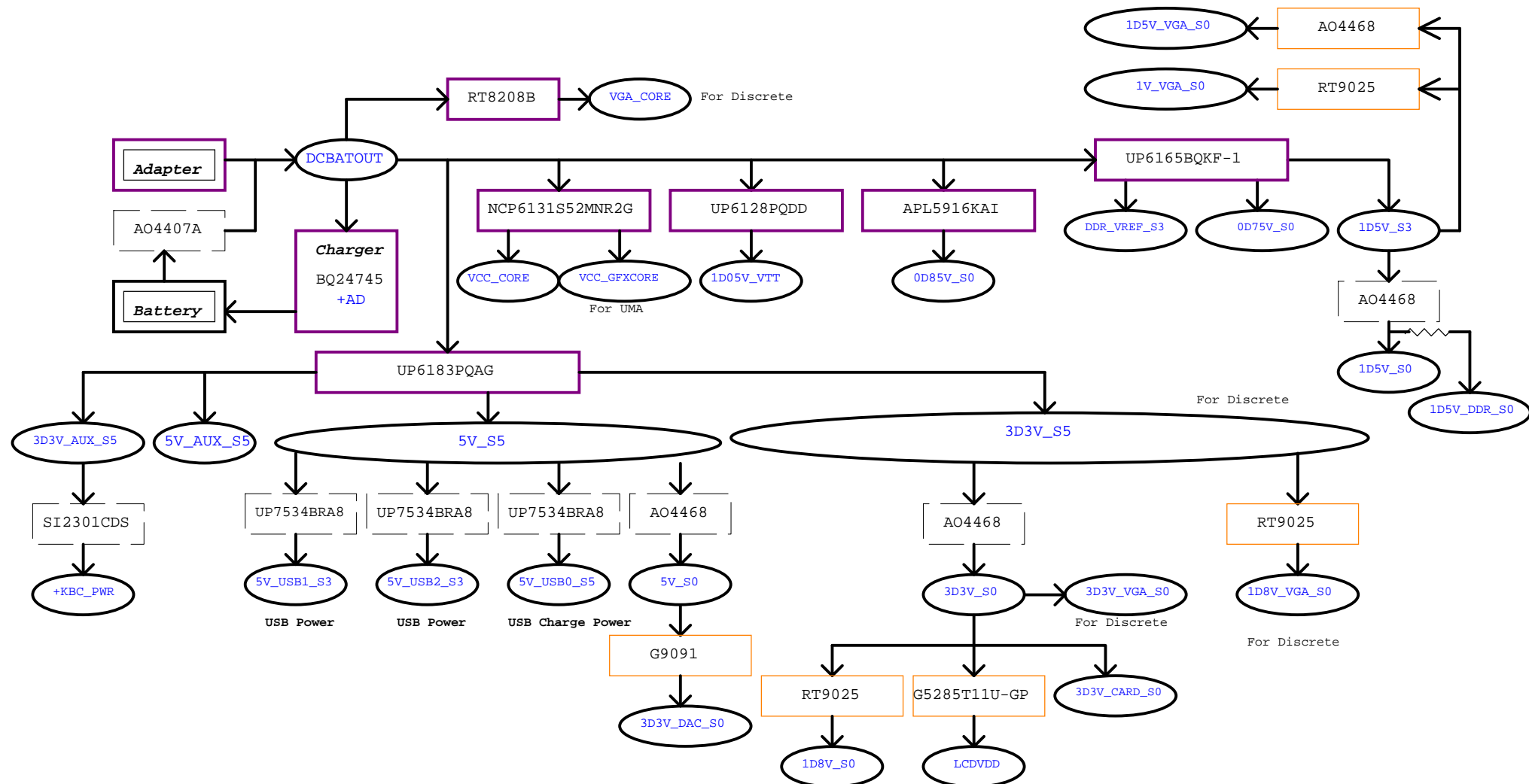
Power Sequence



(AC mode)

red word: KBC GPIO

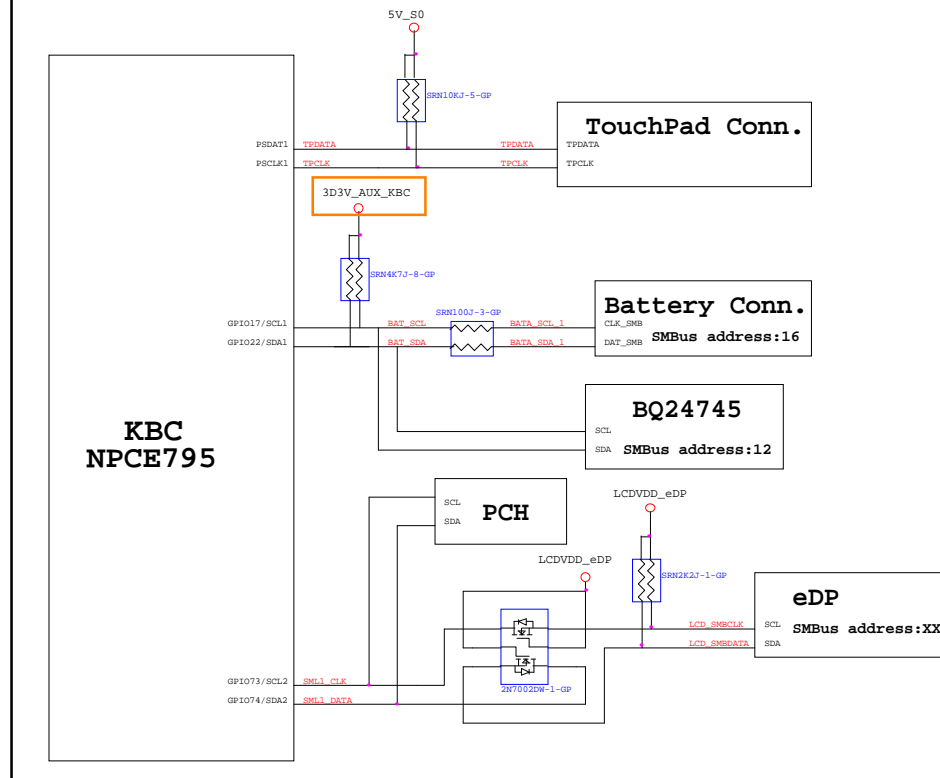




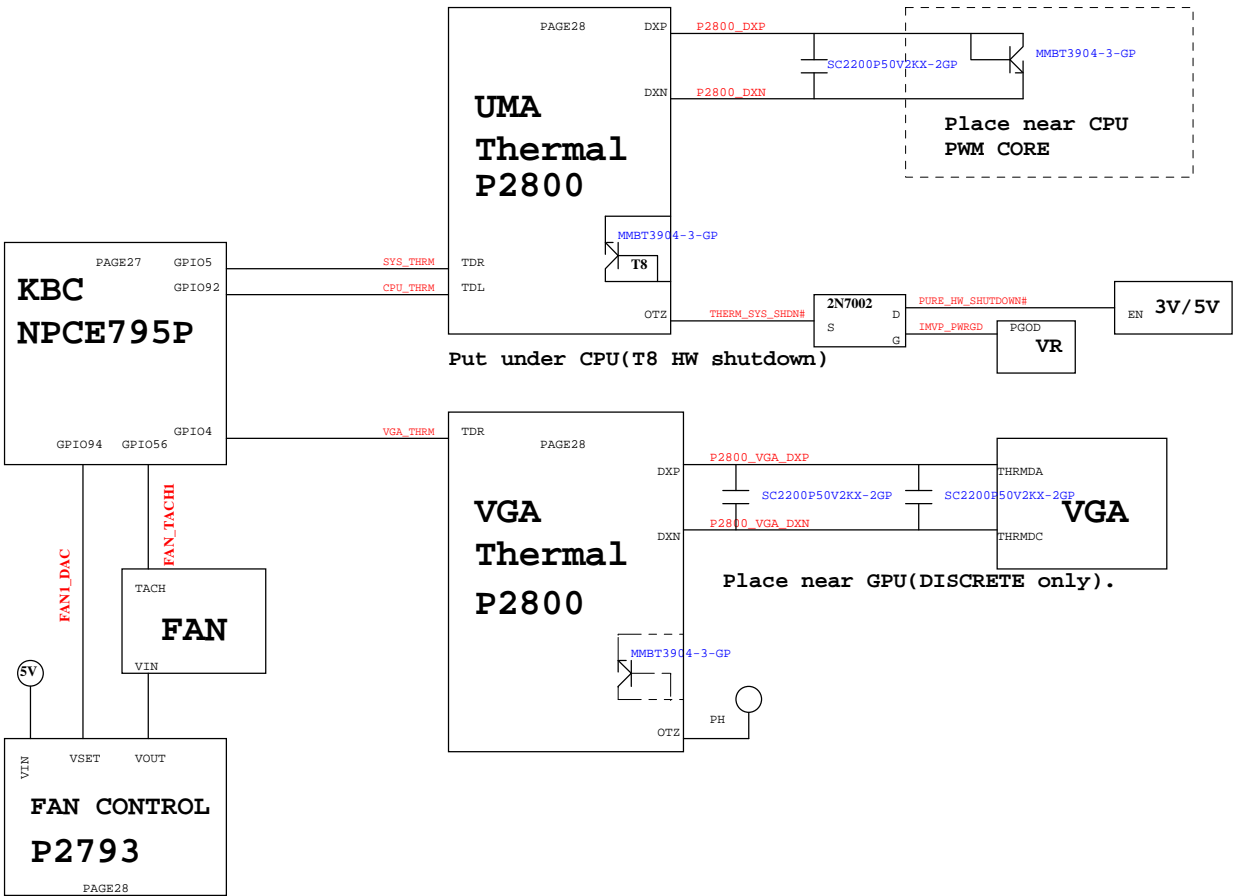
Power Shape



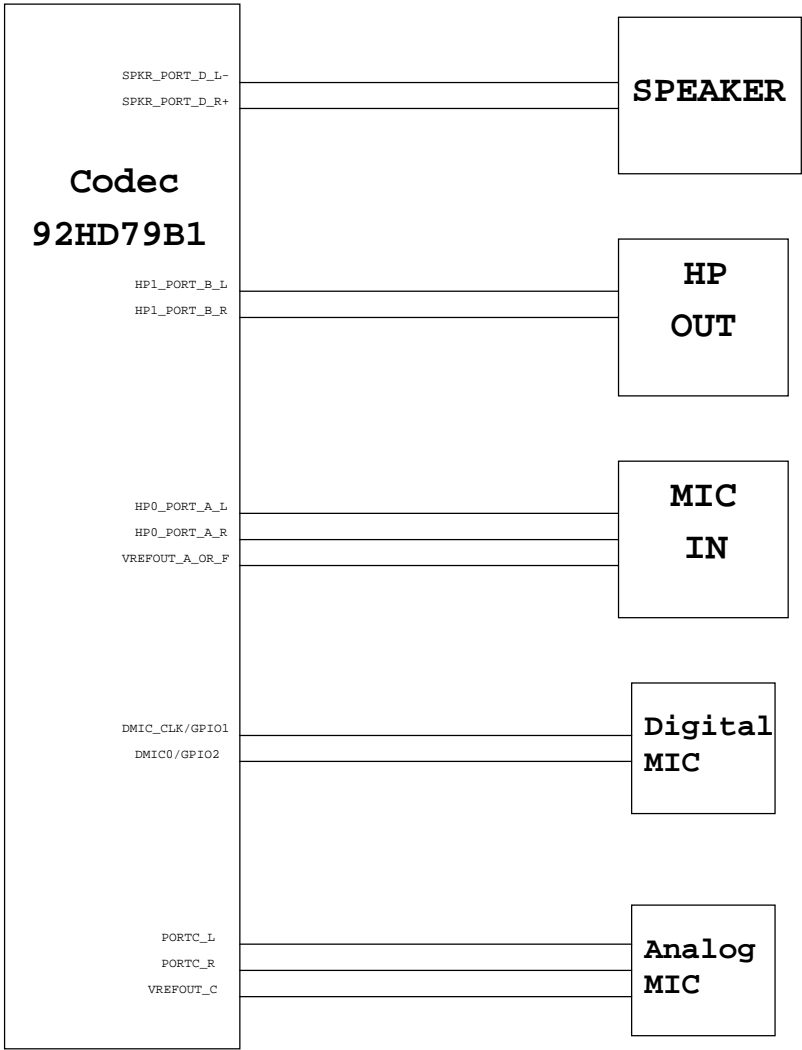
KBC SMBus Block Diagram

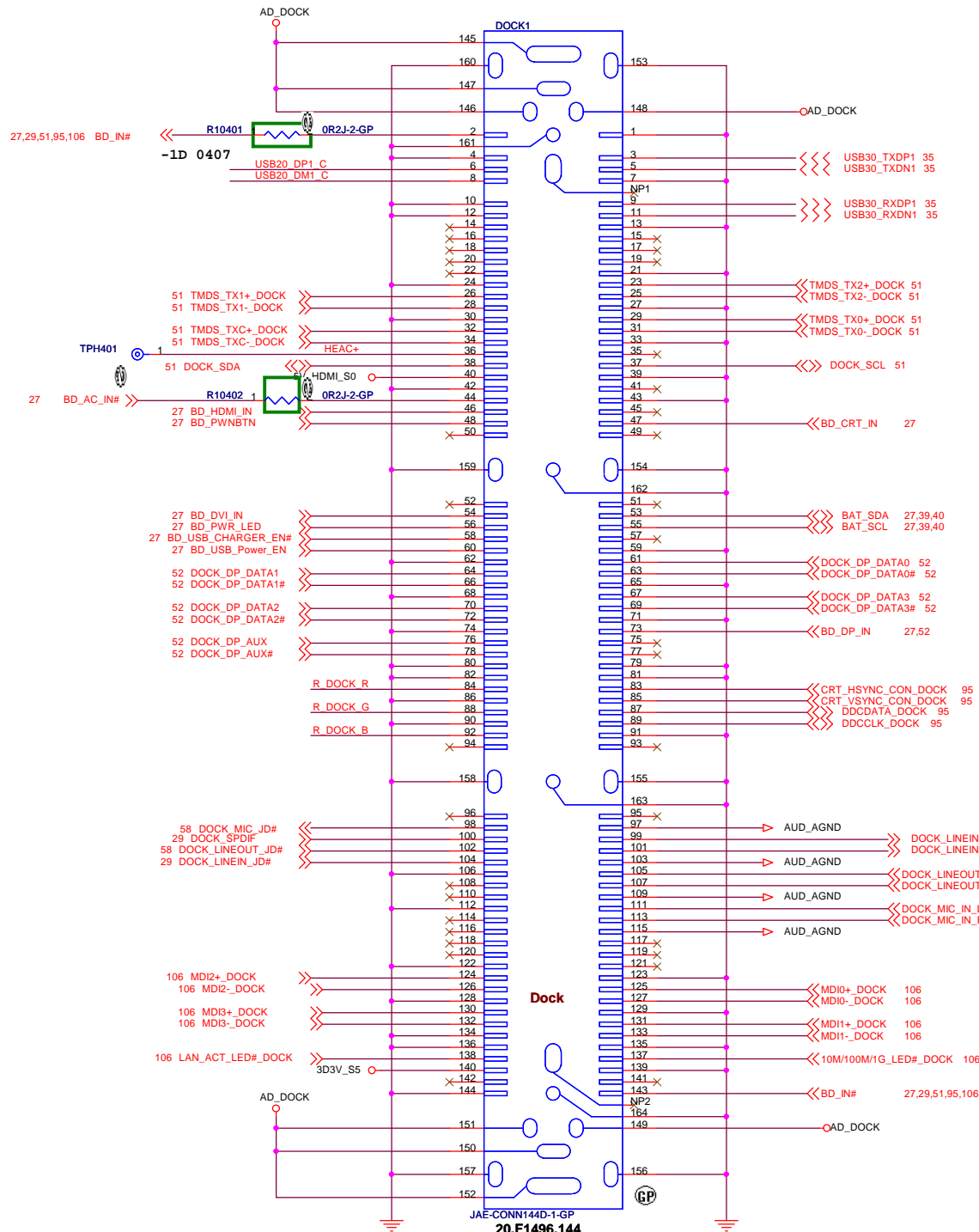


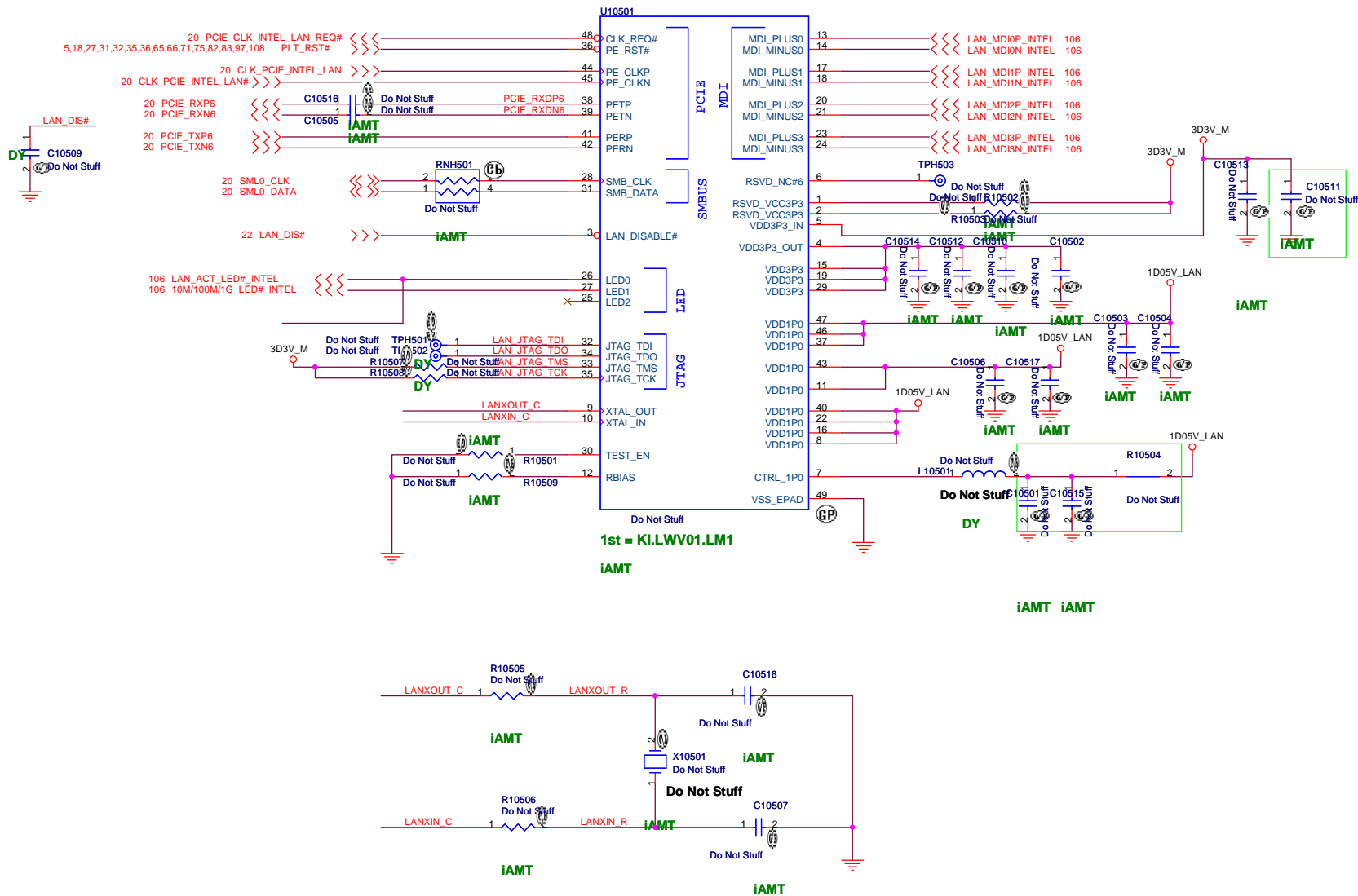
Thermal Block Diagram



Audio Block Diagram



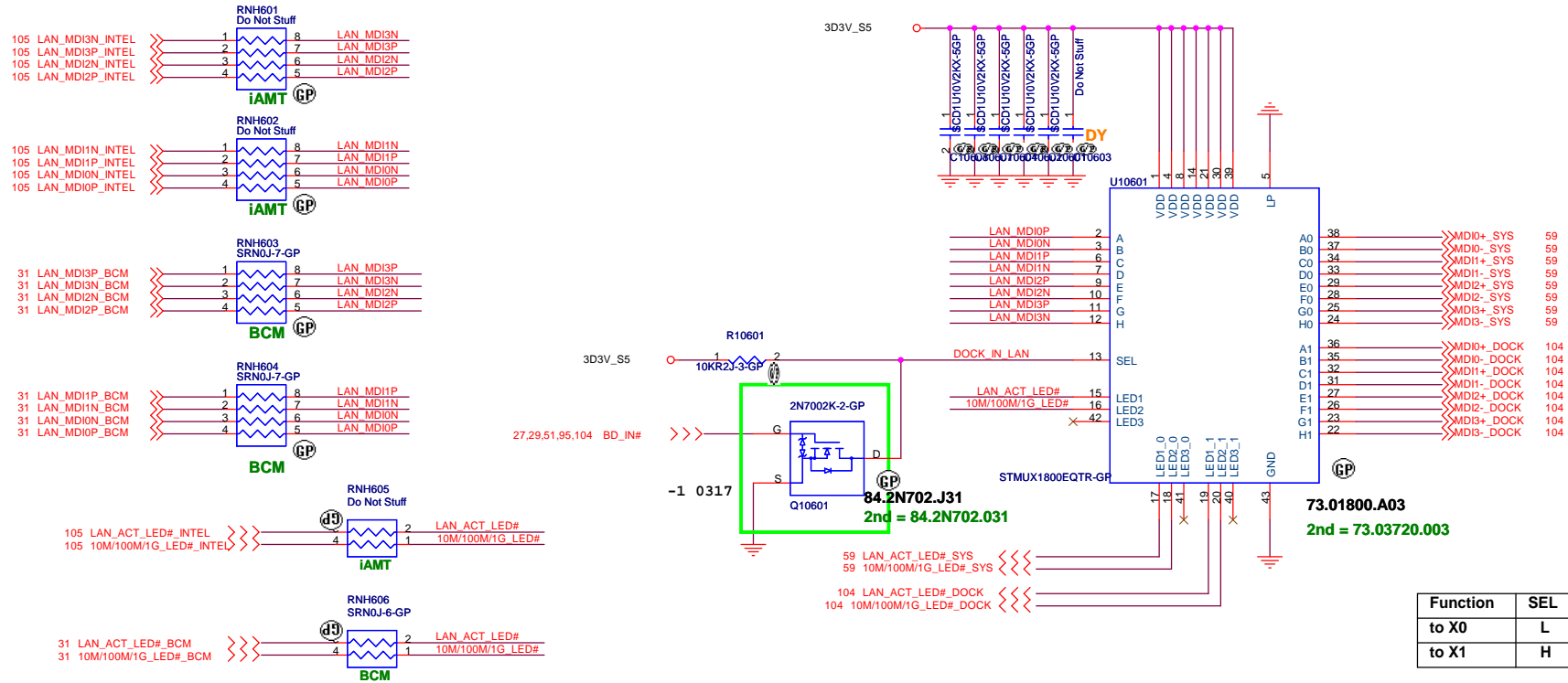




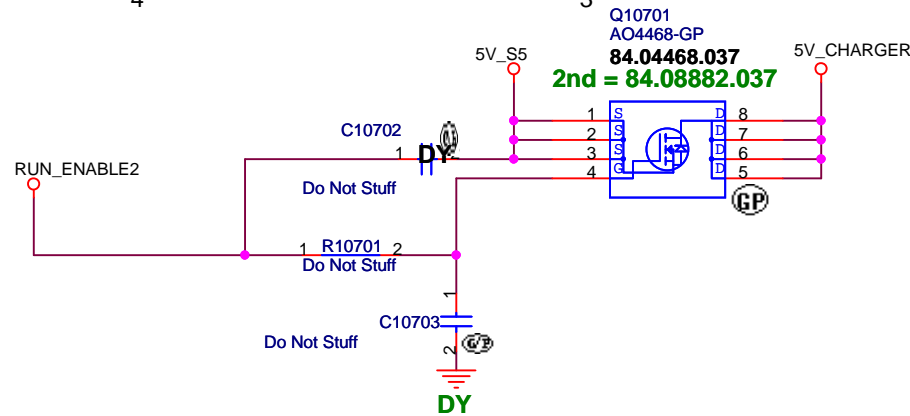
D12G

緯創資通		Wistron Corporation	
		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
LAN INTEL 82579			
Size	Document Number	Rev	
A3	BA40-HR	SD	
Date:	Thursday, April 07, 2011	Sheet	105 of 109

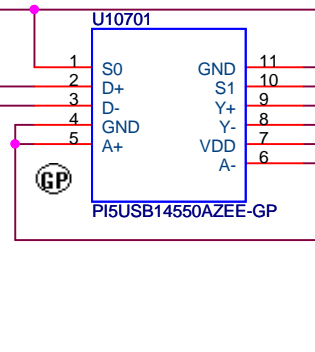
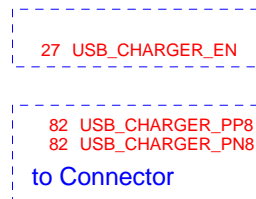
LAN switch



Function	SEL	
to X0	L	SYSTEM
to X1	H	DOCK



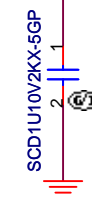
From KBC



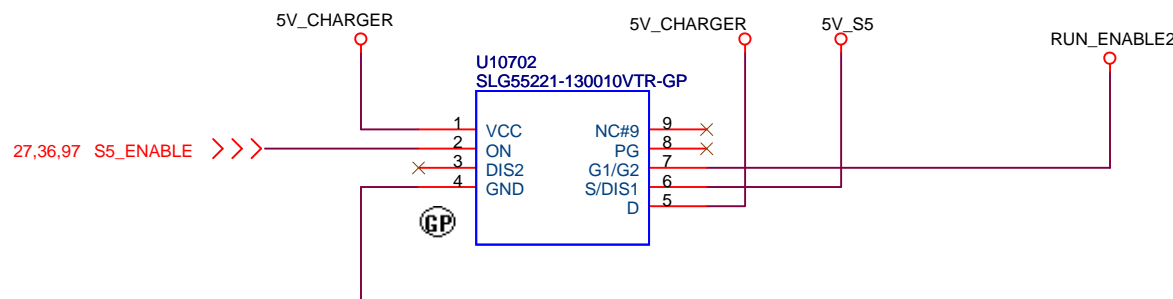
From PCH

USB_PP8 18
USB_PN8 18

5V_CHARGER



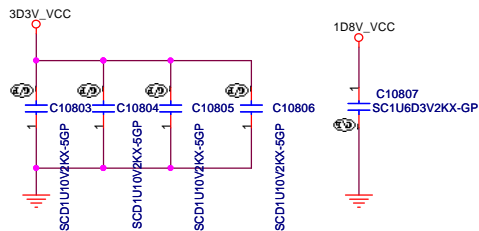
C10701



D12G

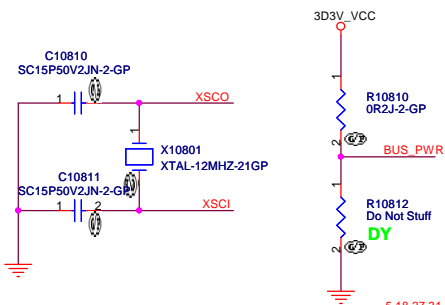
<div>緯創資通</div> <div>Wistron Corporation</div> <div>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</div>	
Title	
USB charger	
Size A4	Document Number BA50V-HR
Date: Thursday, April 07, 2011	Rev SD
Sheet 107	of 109

WWW.ALISALER.COM

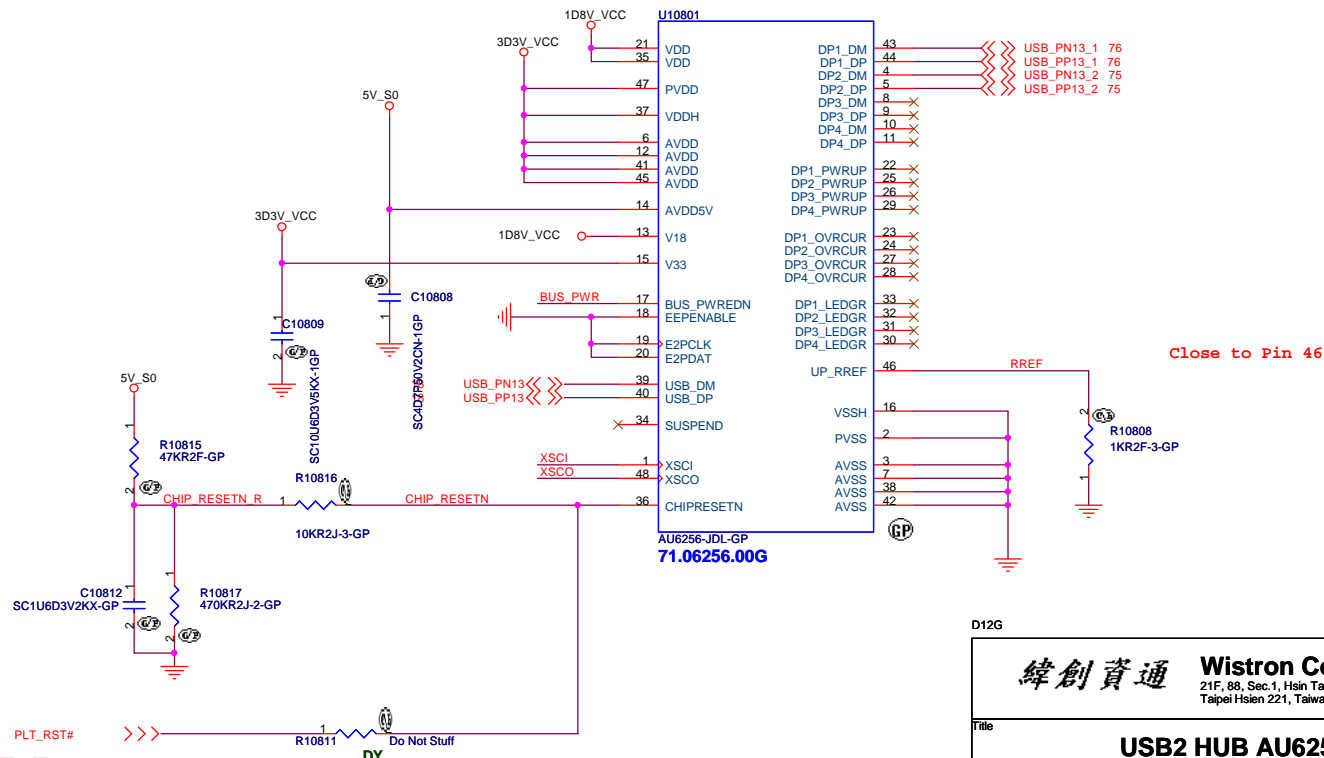


	Port1	Port2	Port3	Port4
R20,R31,R33=>0 ohm	Normal	Normal	Normal	Normal
R19,R32,R34=>NC	Removable	Removable	None	None
R20,R32,R34=>0 ohm	Removable	Removable	None	None
R19,R31,R33=>NC	non-removable	non-removable	None	None
R20,R31,R34=>0 ohm	non-removable	non-removable	None	None
R19,R32,R33=>NC	non-removable	Removable	Removable	None
R20,R32,R33=>0 ohm	non-removable	Removable	Removable	None
R19,R31,R34=>NC				

EEPENABLE
 0 : Use Internal Rom
 1 : Use External Rom



5,18,27,31,32,35,36,65,66,71,75,82,83,97,105 PLT_RST#

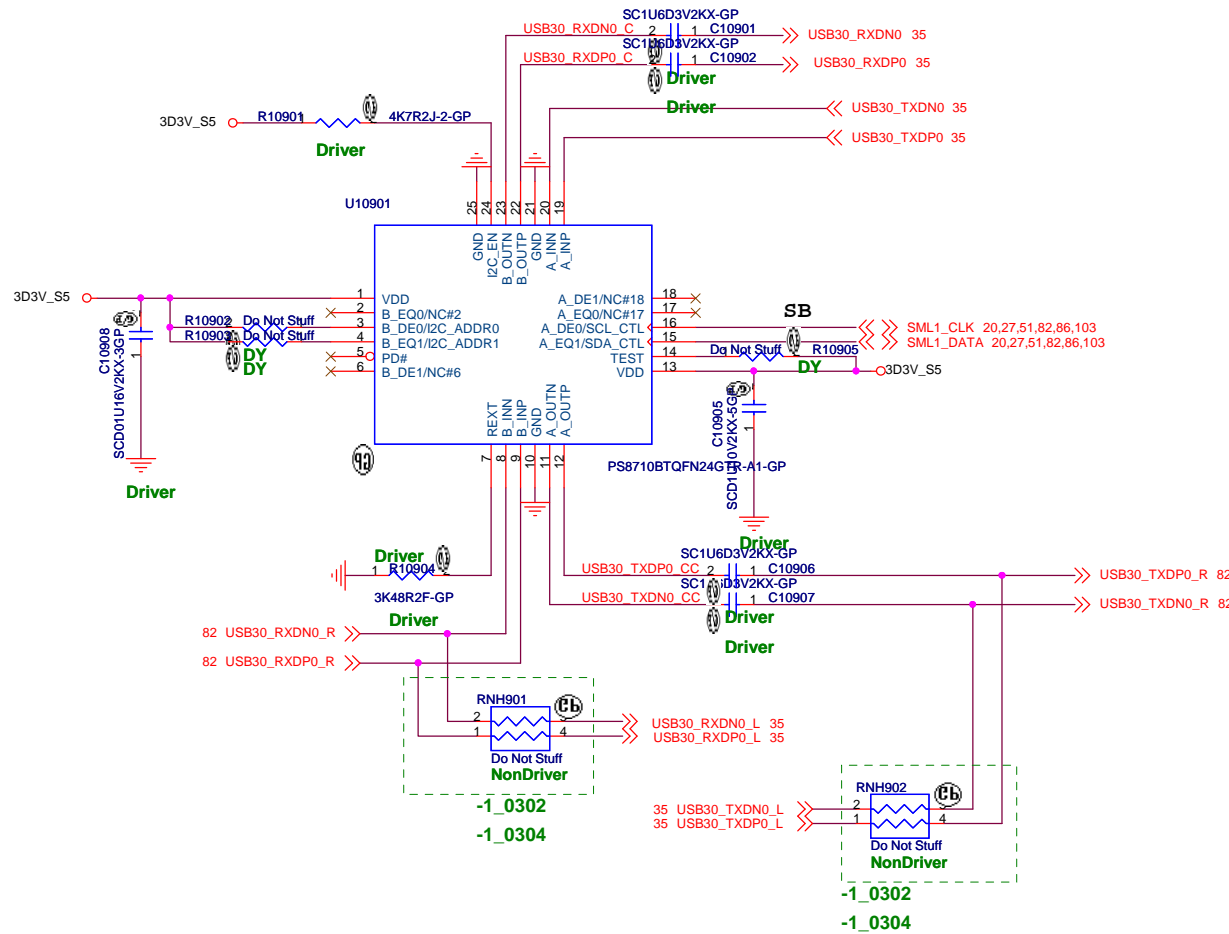


D12G

緯創資通 Wistron Corporation
 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
 Taipei Hsien 221, Taiwan, R.O.C.

Title: **USB2 HUB AU6256**
 Size: Document Number: **BAD50-HR** Rev: **SD**
 Date: Thursday, April 07, 2011 Sheet 108 of 109

I2C mode To USB BD



D12G

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title			USB30 re-driver
Size	Document Number	Rev	SD
B	BAD50-HR		
Date:	Thursday, April 07, 2011	Sheet	109 of 109